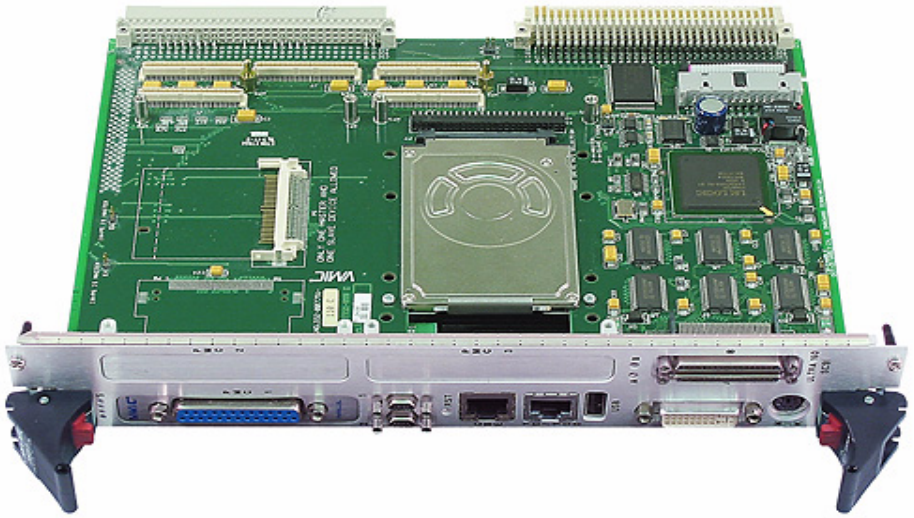
GE
Intelligent Platforms

Hardware Reference

VMIVME-7851*/VME-7851RC*
Intel® Pentium® 4 Processor M-Based
VME Single Board Computer

THE VMIVME-7851 IS DESIGNED TO MEET THE EUROPEAN UNION (EU) RESTRICTION OF HAZARDOUS SUBSTANCE (ROHS) DIRECTIVE (2002/95/EC) CURRENT REVISION.



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January 10, 2013

Waste Electrical and Electronic Equipment (WEEE) Returns

GE is registered with an approved Producer Compliance Scheme (PCS) and, subject to suitable contractual arrangements being in place, will ensure WEEE is processed in accordance with the requirements of the WEEE Directive.

GE will evaluate requests to take back products purchased by our customers before August 13, 2005 on a case by case basis. A WEEE management fee may apply.

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Overview

GE VMIVME-7851*/VME-7851RC* are full-featured Pentium® 4 Processor M-based single board computers (SBCs) in dual slot, passively cooled, Eurocard form factors. These SBCs utilize the advanced technology of Intel®'s 852GM chipset running a front-side bus rate of 400 MHz. The VMIVME-7851/ VME-7851RC are compliant with the VMEbus Specification Rev. C.1 and feature a transparent PCI-to-VME bridge, allowing the boards to function as a system controller or peripheral CPU in multi-CPU systems.

Desktop Features

The VMIVME-7851/VME-7851RC main boards provide features typically found on desktop systems such as:

- Up to 1 GByte PC1600 DDR SDRAM
- Built-in SVGA and DVI support with 4 MByte DRAM display cache
- Two built-in Ethernet controllers (one supporting Gigabit Ethernet, the other supporting 10/100 Mbit Ethernet)
- IDE drive support
- Floppy drive support
- Two high-performance 16550-compatible serial ports
- Front Panel USB port Rev. 2.0
- Real-Time clock/calendar
- Front panel reset switch
- Miniature speaker
- Keyboard/Mouse port

The expansion boards use the second VME slot and add the following capabilities:

- Ultra160 SCSI dual-channel (optional)
- Two additional PMC sites (#2 and #3)
- Hidden CompactFlash (Type I or II)
- 1.8” IDE hard drive (this option leaves PMC site open)
- 2.5” IDE hard drive (this option blocks the PMC slot but provides better performance)
- One parallel port (full size, DB25)

The VMIVME-7851/VME-7851RC are capable of executing many of today’s desktop operating systems such as Microsoft®’s Windows® 2000, Windows XP and a wide variety of Linux®-based operating systems. The standard desktop features of the VMIVME-7851/VME-7851RC are described in **Chapter 2** of this manual.

Embedded Features

The VMIVME-7851/VME-7851RC provide features useful to embedded applications such as:

- I^2C bus support
- Remote Ethernet booting
- Up to 1 GByte of bootable CompactFlash (optional)
- Four general-purpose programmable timers (two 16-bit and two 32-bit)
- Software-selectable Watchdog Timer with reset
- 32 KByte Non-volatile SRAM

Additionally, the VMIVME-7851/VME-7851RC offer three PMC expansion sites with front-panel access. The VMIVME-7851/VME-7851RC are capable of executing many of today's embedded operating systems such as VxWorks®, QNX®, LynxOS® and Microsoft's Windows XP. The embedded features of the VMIVME-7851/VME-7851RC are described in **Chapter 3** of this manual.

The VMIVME-7851/VME-7851RC are suitable for use in a variety of applications, such as: telecommunications, simulation, instrumentation, industrial control, process control and monitoring, factory automation, automated test systems, data acquisition systems and anywhere that the highest performance processing power in a dual VME slot is desired.

Intel 852GM Chipset

The VMIVME-7851/VME-7851RC incorporate the latest Intel 852GM chipset technology. The Intel 852GM chipset is an optimized integrated graphics solution with a 400 MHz system bus and integrated 32-bit 3D core at 133 MHz with dynamic video memory technology (DVMT). The chipset has a low power design, advanced power management, supporting up to 1 GByte of DDR system memory. The 852GM is a Graphics Memory Controller Hub component (GMCH), providing the processor interface, system memory interface (DDR SDRAM), Hub interface, CRT and digital video out (DVO) port.

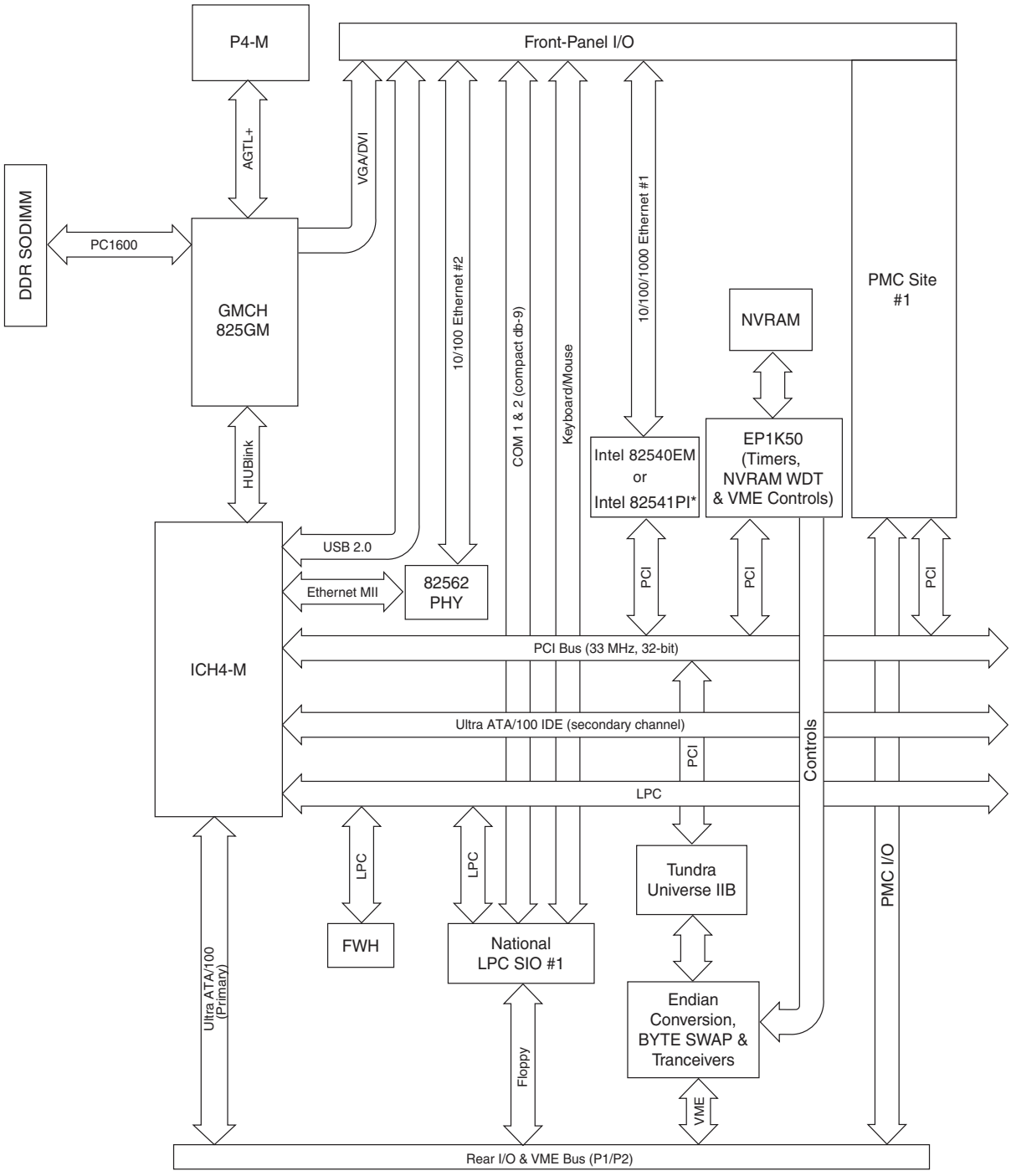
Key features for the 852GM:

- 400 MHz Processor system bus controller
- Graphics controller interface
- Analog and Digital video output ports
- Supports DDR200 memory technology

Highspeed accelerated hub architecture interface for communication with the ICH4-M (I/O controller).

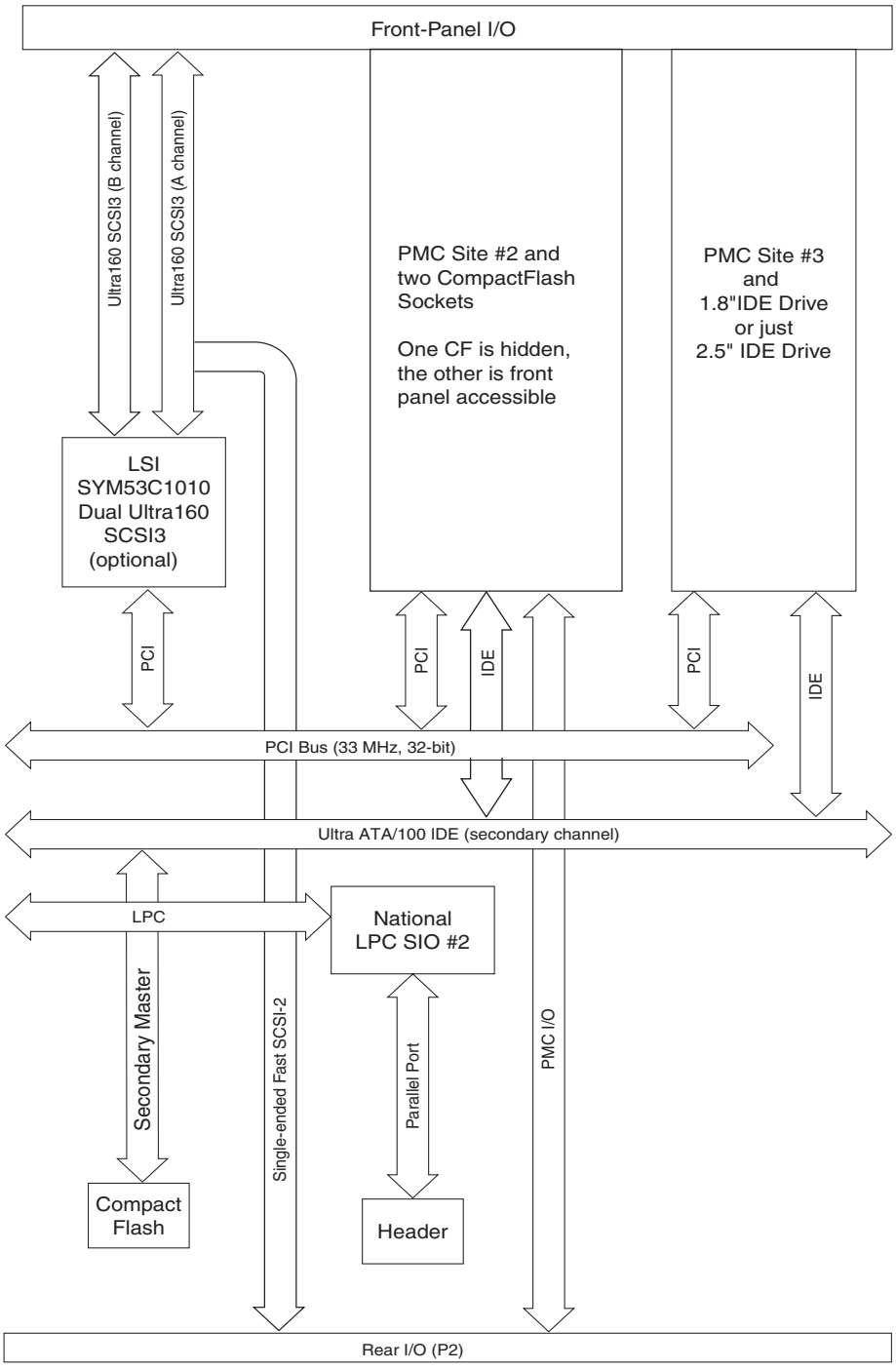
Block Diagram of Main Board

Figure 1 VMIVME-7851/VME-7851RC Block Diagram (Main Board)



Block Diagram of Expansion Board

Figure 2 VMIVME-7851/VME-7851RC Block Diagram (Expansion Board)



Notation and Terminology

This product bridges the traditionally divergent worlds of Intel-based PCs and Motorola-based VME controllers; therefore, some confusion over "conventional" notation and terminology may exist. Every effort has been made to make this manual consistent by adhering to conventions typical for the Motorola/VME world; nevertheless, users in both camps should review the following notes:

- Hexadecimal numbers are listed Motorola-style, prefixed with a dollar sign: $F79, for example. By contrast, this same number would be signified 0F79H according to the Intel convention, or 0xF79 by many programmers. Less common are forms such as $F79_h$ or the mathematician's $F79_{16}$.
- An 8-bit quantity is termed a "byte," a 16-bit quantity is termed a "word," and a 32-bit quantity is termed a "longword." The Intel convention is similar, although their 32-bit quantity is more often called a "doubleword."
- Motorola programmers should note that Intel processors have an I/O bus that is completely independent from the memory bus. Every effort has been made in the manual to clarify this by referring to registers and logical entities in I/O space by prefixing I/O addresses as such. Thus, a register at "I/O $140" is not the same as a register at "$140," since the latter is on the memory bus while the former is on the I/O bus.
- Intel programmers should note that addresses are listed in this manual using a linear, "flat-memory" model rather than the old segment:offset model associated with Intel Real Mode programming. Thus, a ROM chip at a segment:offset address of C000:0 will be listed in this manual as being at address $C0000. For reference, here are some quick conversion formulas:
  - Segment:Offset to Linear Address
  - Linear Address = (Segment × 16) + Offset
  - Linear Address to Segment:Offset
  - Segment = ((Linear Address ÷ 65536) - remainder) × 4096
  - Offset = remainder × 65536
  - Where remainder = the fractional part of (Linear Address ÷ 65536)

NOTE

There are many possible segment:offset addresses for a single location. The formula above will provide a unique segment:offset address by forcing the segment to an even 64 KByte boundary, for example, $C000, $E000, etc. When using this formula, make sure to round the offset calculation properly!

Organization

This manual is composed of the following chapters and appendices:

Chapter 1 - Installation and Setup describes unpacking, inspection, hardware jumper settings, connector definitions, installation, system setup and operation of the VMIVME-7851/VME-7851RC.

Chapter 2 - Standard Features describes the unit design in terms of the standard PC memory and I/O maps, along with the standard interrupt architecture.

Chapter 3 - Embedded PC/RTOS Features describes the unit features that are beyond standard functions.

Chapter 4 - Optional Features describes optional additional capabilities beyond those of a typical IBM PC/AT-compatible CPU.

Maintenance provides information relative to the care and maintenance of the unit.

Compliance provides applicable information regarding regulatory compliance.

Appendix A - Connector Pinouts illustrates and defines the connectors included in the unit's I/O ports.

Appendix B - System Driver Software provides details for installing drivers under Windows 2000 and Windows XP.

Appendix C - Argon BIOS describes the menus and options associated with the Argon BIOS.

Appendix D - SCSI BIOS presents general information about the SDMS SCSI BIOS and Configuration Utility Version 4.19.00.

Appendix E - AMI BIOS Setup Utility describes the menus and options associated with the American Megatrends, Inc. (system) BIOS.

References

Pentium 4 Processor-M µFCPGA package at 1.7 to 2.2GHz
January 2003, Order Number 250686-005

Intel 852GM Graphics and Memory Controller Hub (GMCH)
January 2003, Order Number 252338-001

Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)
January 2003, Order Number 252337-001

PCI Local Bus Specification, Rev. 2.1
PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214
(800) 433-5177 (U.S.)
(503) 797-4207 (International)
(503) 234-6762 (FAX)

PC87366 128-Pin LPC Super I/O with System Hardware Monitoring, MIDI and Game Ports
National Semiconductor
2900 Semiconductor Dr.
P.O. Box 58090
Santa Clara, CA 95052-8090
(800) 272-9959
(800) 737-7018 (FAX)

LSI SYM53C1010 Dual SCSI Controller
LSI Logic Corp.
1551 McCauthy Blvd.
Milpitas, CA 95035
(866) 574-5741
www.symbios.com

CMC Specification, P1386/Draft 2.0 from:
IEEE Standards Department
Copyrights and Permissions
445 Hoes Lanes, P.O. Box 1331
Piscataway, NJ 08855-1331, USA

PMC Specification, P1386.1/Draft 2.0 from:

IEEE Standards Department
Copyrights and Permissions
445 Hoes Lanes, P.O. Box 1331
Piscataway, NJ 08855-1331, USA

VMISFT-9420 IOWorks Access User's Guide
Doc. No. 520-009420-910
GE
12090 South Memorial Pkwy.
Huntsville, AL 35803-3308
(800) 322-3616
www.ge-ip.com

GE Tundra Universe II Based VMEbus Interface
Doc. No. 500-000211-000
GE
12090 South Memorial Pkwy.
Huntsville, AL 35803-3308
(800) 322-3616
www.ge-ip.com

For a detailed description and specification of the VME bus, please refer to:

VMEbus Specification Rev. C. and the VMEbus Handbook
VMEbus International Trade Assoc. (VITA)
7825 East Gelding Dr.
Suite 104
Scottsdale, AZ 85260
(602) 951-8866
(602) 951-0720 (FAX)
www.vita.com

The following is useful information related to the operation of the I^2C controllers:

The I^2C Specification version 2.0
Philips Semiconductor
811 East Arques Ave.
Sunnyvale, CA 94088-3409
(800) 234-7381
www.semiconductors.philips.com

Safety Summary

The following general safety precautions must be observed during all phases of the operation, service and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product.

GE assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to GE for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this system.
Use extreme caution when handling, testing and adjusting.

Warnings, Cautions and Notes

WARNING

WARNING denotes a hazard. It calls attention to a procedure, practice, or condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION

CAUTION denotes a hazard. It calls attention to an operating procedure, practice, or condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE

NOTE denotes important information. It calls attention to a procedure, practice, or condition which is essential to highlight.

TIP

Tip denotes a bit of expert information.

LINK

This is link text.

1 • Installation and Setup

This chapter describes the hardware switch settings, connector descriptions, installation, system setup and operation of the VMIVME-7851/VME-7851RC.

1.1 Unpacking Procedures

Any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to GE Customer Care along with a request for advice concerning the disposition of the damaged item(s).

CAUTION

Some of the components assembled on GE products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

1.2 Hardware Setup

The VMIVME-7851/VME-7851RC are factory populated with user-specified options as part of the VMIVME-7851/VME-7851RC ordering information. For option upgrades or for any type of repairs, contact customer care to receive a Return Material Authorization (RMA).

GE Customer Care is available at:
1-800-433-2682, 1-780-401-7700.

Or, visit our website **www.ge-ip.com**

The VMIVME-7851/VME-7851RC are tested for system operation and shipped with factory-installed header jumpers. The physical locations of the switches and connectors for the SBC with the PMC option are illustrated in **Figure 1-1 on page 22** and **Figure 1-2 on page 23**. The definitions of the connectors, headers and switches are included in **Table 1-1 on page 24** through **Table 1-8 on page 26**.

CAUTION

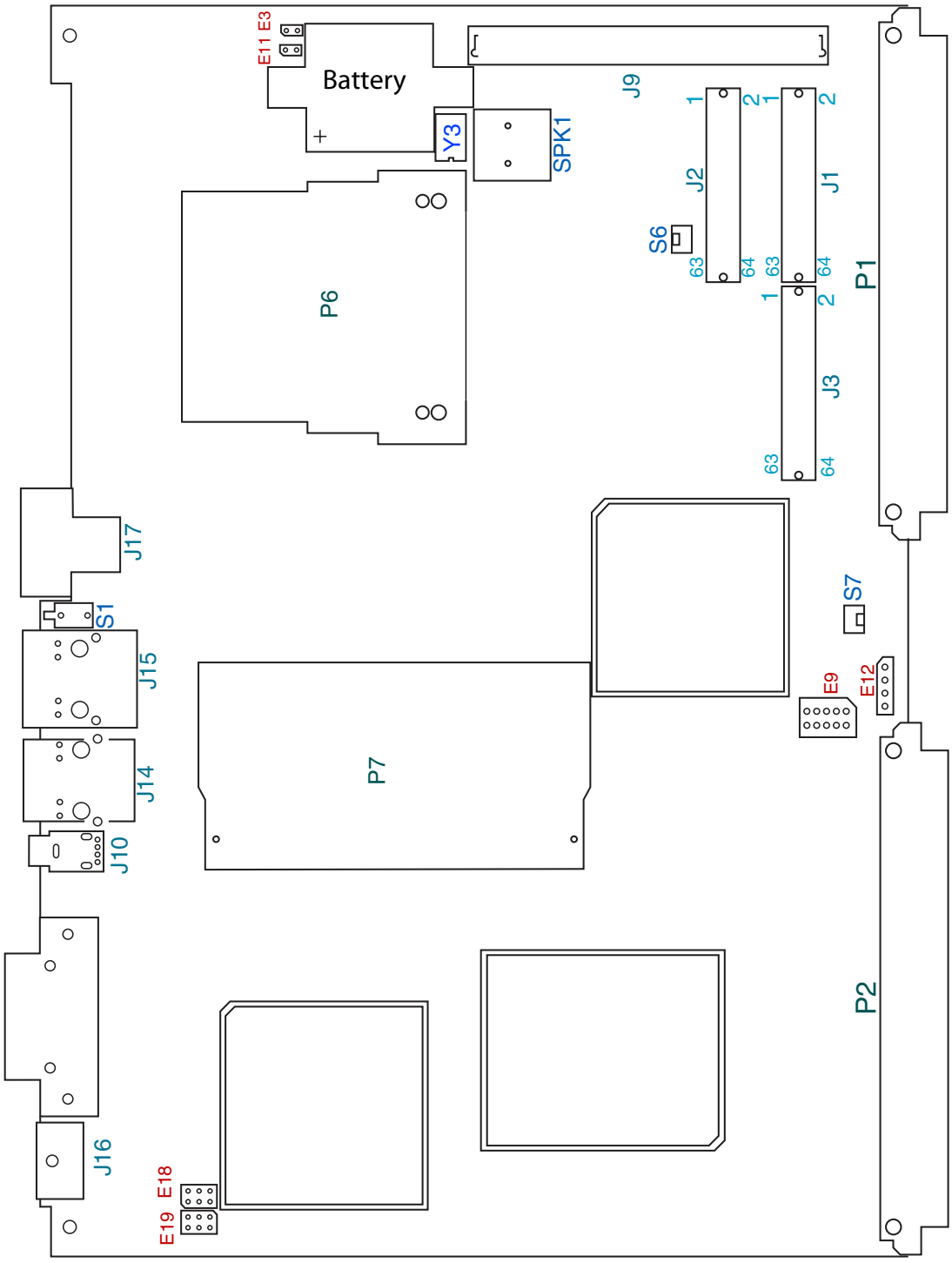
All jumpers marked *User Configured* in the following tables may be changed or modified by the user. All jumpers marked *Factory Configured* should not be modified by the user.

Care must be taken when making jumper modifications to ensure against improper settings or connections. Improper settings may result in damage to the unit.

Modifying any jumper not marked *User Configured* will void the Warranty and may damage the unit.

1.3 Main Board PMC and Jumper Locations

Figure 1-1 VMIVME-7851/VME-7851RC (Main Board) PMC and Jumper Locations



1.4 (Expansion Board) PMC and Jumper Locations

Figure 1-2 VMIVME-7851/VME-7851RC (Expansion Board) PMC and Jumper Locations

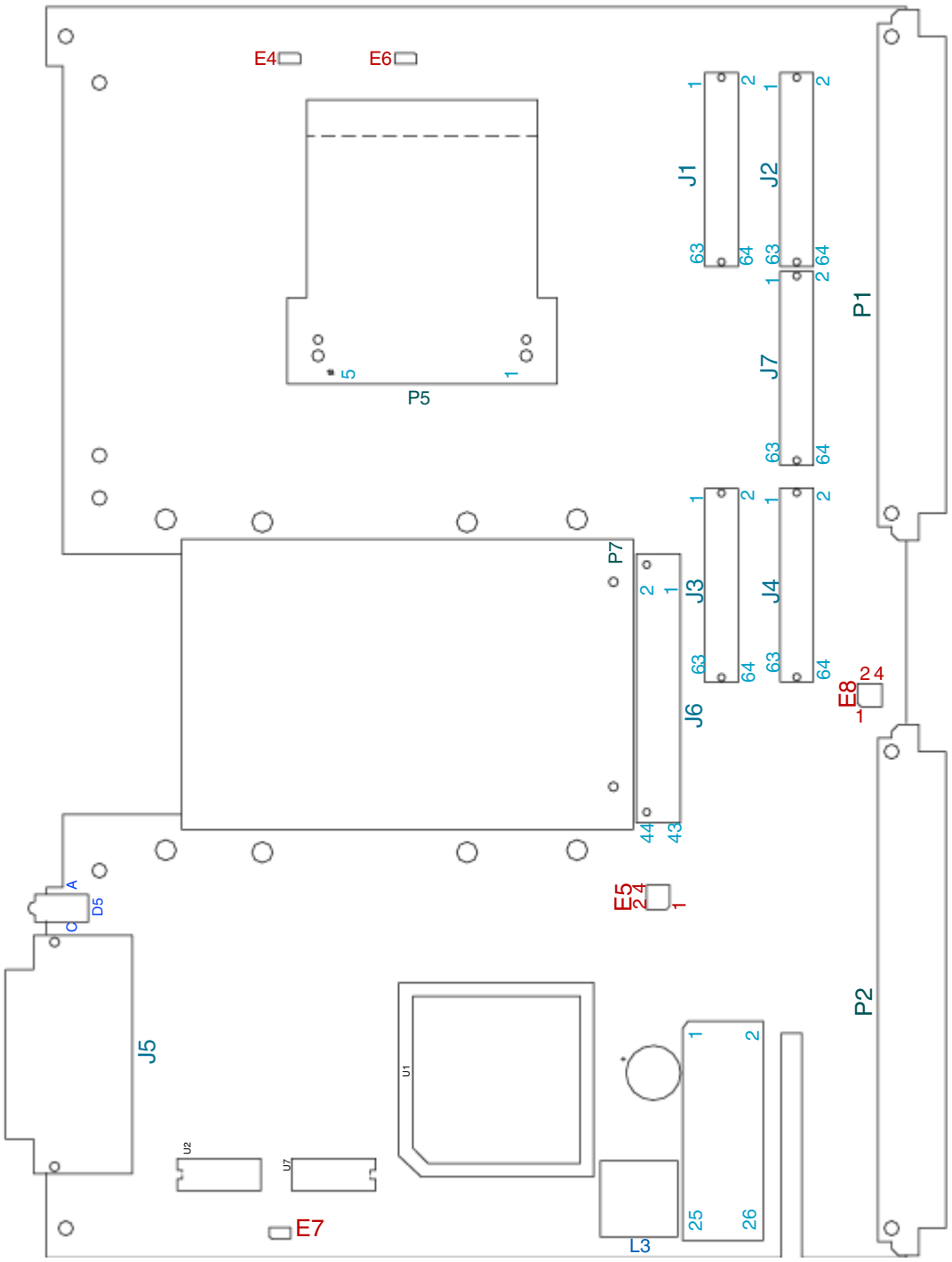


Table 1-1 SBC Connectors

Connector (Main Board)	Function
J16	Mouse/Keyboard
J14, J15	Ethernet 1 & 2
P2, J9 to Expansion Board	IDE (PRI), Floppy
J12	USB
J10	Video
E9, E10, E18, E19	Factory Reserved Do Not Use
J9	Board to Board Connector
E12	I^2C Header
J1, J2, J3	PMC Slot 1
J17	COM 1, COM 2
P1, P2	VME
P6	Type I/II CompactFlash
Connector (Expansion Board)	Function
J1, J2, J7	PMC #2
J3, J4	PMC #3
P1	VME (Power)
P2	VME (Power), PMC I/O and SCSI
P3	Board-to-Board Connector
P4	Parallel Port (25 pin IDC)
P5	"Hidden" type I/II CompactFlash
P6	"Accessible" type I/II CompactFlash
P7	1.8" IDE Drive (optional)
J5	Dual Ultra160 SCSI (optional)
J6	2.5" IDE Drive (optional)
E4, E5, E6	IDE Secondary Master/Slave Selection
E7	Onboard SCSI Termination for Channel A
E8	PMC #2 I/O for J7 pins 49, 55, 57 and 59

NOTE

The BIOS has the capability (not currently enabled) of password protecting casual access to the unit's CMOS set-up screens. The Password Clear jumper allows the user to clear the password in the case of a forgotten password.

To clear the CMOS password:

1. Turn off power to the unit.
2. Momentarily short the pins of E3 for approximately five seconds.
3. Power up the unit.

When power is reapplied to the unit, the CMOS password will be cleared.

Table 1-2 Password Clear (User Configurable) - Jumper (E3)

Select	Jumper Position
Normal	**Open**
Clear CMOS/Password	Momentarily Short

Table 1-3 VME Switch (User Configurable) - Switch (S7)

Select	Switch Position	Switch Number
Enable SYSFAIL Generation	**On**	**1**
Map UNIV2 to I/O Space	**On**	**2**

Table 1-4 VME Switch (User Configurable) - Switch (S6)

Select	Switch Position	Switch Number
Enable VME SYSRESET Driver	**On**	**1**
Enable SYSRESET Receiver	**On**	**2**

1.4.1 Expansion Board Jumpers

Table 1-5 Secondary IDE Connector P6 Master/Slave (User Configurable) - Jumper (E4)

Select	Jumper Position
P6 is Master	In
P6 is Slave	**Out**

Table 1-6 Secondary IDE Connector J6/P7 Hard Drive (User Configurable) - Jumper (E5)

Select	Jumper Position
Hard Drive is Master	**2-4 or Out**
Hard Drive is Slave	3-4 (for Toshiba)
* Other hard drive vendors' jumper settings may vary.	

Table 1-7 Secondary IDE Connector P5 Master/Slave (User Configurable) - Jumper (E6)

Select	Jumper Position
P5 is Master	In
P5 is Slave	**Out**

Table 1-8 SCSI Channel A (User Configurable) - Jumper (E7)

Select	Jumper Position
Enable Termination	**In**
Disable Termination	Out

NOTE

Jumpers E4, E5 and E6 will be configured differently for each hardware load option. Only two devices allowed per channel.

1.4.2 Power Requirements

The VMIVME-7851/VME-7851RC require +5 V, +12 V and -12 V from the VME backplane. Below are the voltage and current requirements.

Supply	Current (Typical)	Current (Maximum)
+5 V	4A	12.5A
+12 V	105mA	200mA
-12 V	50mA	75mA

The VMIVME-7851/VME-7851RC provide power to the PMC site in accordance with the PMC specification. The maximum current provided on the +5 V supply is 1.5A per PMC site. The maximum current provided on the +3.3 V supply is 2.3A per PMC site.

The +12 V and -12 V supplies are provided to the PMC site and to the rear transition modules (RTMs) (such as the VMIACC-0562*/ACC-0562RC* RTMs). The total +12 V or -12 V current provided to the VMIVME-7851/VME-7851RC (as indicated above), the PMC site and the RTMs must not exceed 750mA each, in accordance with the VMEbus Specification.

1.5 Installation

The VMIVME-7851/VME-7851RC conform to the VME physical specification for a dual slot 6U Eurocard. It can be plugged directly into any standard chassis accepting this type of board.

CAUTION

Do not install or remove the boards while power is applied.

The following steps describe the GE recommended method for VMIVME-7851/VME-7851RC installation and power-up:

1. Make sure power to the equipment is off.
2. Choose chassis slot. The VMIVME-7851/VME-7851RC must be attached to a dual P1/P2 VME backplane. Both slots must have populated P1/P2 connectors to provide the necessary power pins.

   If the VMIVME-7851/VME-7851RC are to be the VME system controller, choose the first two VME slots. If a different board is the VME system controller, choose any two adjacent slots except slots one and two. The VMIVME-7851/VME-7851RC do not require jumpers for enabling/disabling the system controller function.

NOTE

Air flow requirement as measured at the output side of the heatsink is to be greater than 350LFM.

3. Connect all needed peripherals to the front panel. Each connector is clearly labeled on the front panel, and detailed pinouts are in ***Appendix A: Connector Pinouts***. Minimally, a keyboard and a monitor are required if the user has not previously configured the system.

NOTE

Front and Rear panel connectors are not intended to be connected directly to outdoor cables.

USB, COM, Parallel and DVI ports are not intended to be permanently connected and are normally used for maintenance purposes. Permanently installing these cables may cause EMI interference and affect CE Marking certification. These cables may require the addition of ferrite torroid(s) to meet CE Marking.

4. Apply power to the system. Several messages are displayed on the screen, including names, versions and copyright dates for the various BIOS modules on the VMIVME-7851/VME-7851RC.
5. The VMIVME-7851/VME-7851RC feature a CompactFlash resident on the boards.
6. If an IDE drive is installed, the BIOS Setup program must be run to configure the drive types.
7. If a drive is present, install the operating system according to the manufacturer's instructions.

See ***Appendix B: System Driver Software*** for instructions on installing VMIVME-7851/VME-7851RC peripheral driver software during operating system installation.

1.6 Front/Rear Panel Connectors

The VMIVME-7851/VME-7851RC provide front-panel access to the three PMC expansion sites, the DVI-I connector, both 10/100 Ethernet and Gigabit Ethernet connectors, the manual reset switch, COM 1 and 2, USB, the dual Ultra160 SCSI and the status LEDs. A drawing of the VMIVME-7851/VME-7851RC front-panel is shown in **Figure 1-3** ***LED Definitions*** on page 29. The front-panel connectors and indicators are labeled as follows:

- 10/100 — 10/100 Mbit Ethernet connector
- GBE — Gigabit Ethernet Connector
- DVI-I — Digital/Analog Video Connector
- Parallel — Parallel port
- RST — Manual reset switch
- 1:2 — Two COM ports
- M/K — Dual mouse/keyboard connector
- USB — Dual USB connector
- PMC 1, 2, 3 — Three PMC sites
- S — Status LEDs
- Ultra160 SCSI A&B — Two Ultra160 SCSI channels

The VMIVME-7851/VME-7851RC provide rear I/O support for the following: PMC 1 and 2, Primary IDE drive, Single Ended SCSI and floppy drive. These signals are accessed by the use of RTMs such as the VMIACC-0561* and VMIACC-0562/ ACC-0562RC, which terminate into industry standard connectors.

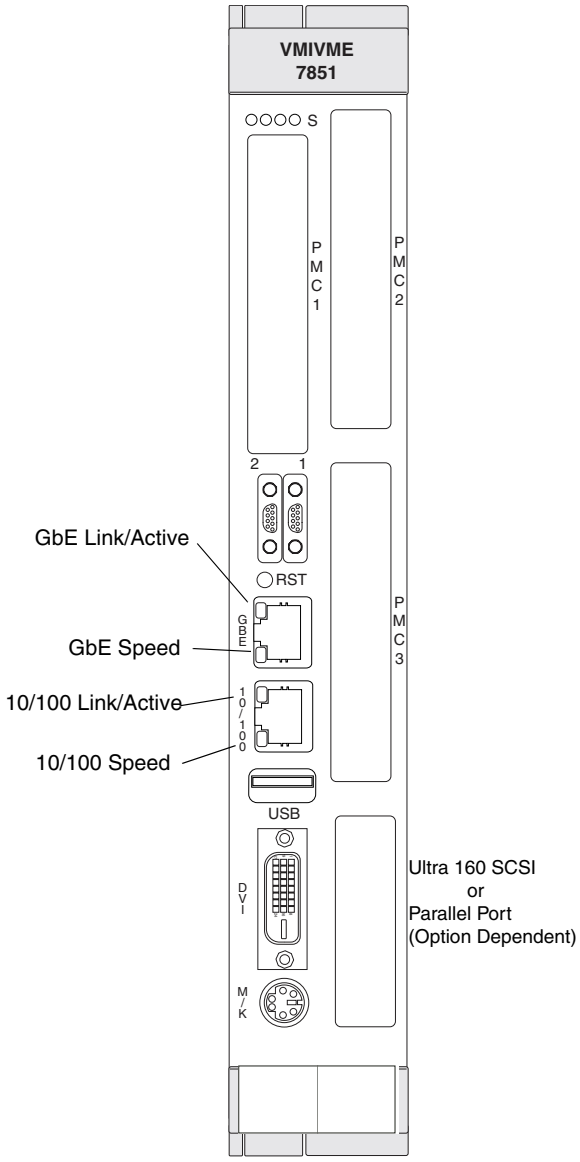
The front panel connectors, including connector pinouts and orientation, for the VMIVME-7851/VME-7851RC are defined in ***Appendix A: Connector Pinouts***. Rear panel connections are defined in the appropriate RTM Installation Guide. Contact Sales for compatible RTMs.

1.6.1 Mouse & Keyboard Port

For a permanently connected mouse/keyboard cable on the VMIVME-7851/ VME-7851RC, a three-turn ferrite torroid (Fair-Rite p/n 2643803B02) is required to be installed as close as possible to its connector port. This is needed in order to meet Class A emissions limits set forth by the EMC Directive for CE Marking (EN55011) and the FCC (47 CFR 15). Alternatively, a clamp-on ferrite (Fair-Rite p/n 0444176451) can be used as long as the three turns are maintained.

1.7 LED Definition

Figure 1-3 LED Definitions



S (Status)	*Reset* - (Leftmost Red LED) Lights during reset conditions. *Power* - (Green LED) Indicates when power is applied to the board. This LED also indicates throttling by blinking slowly. *IDE Indicator* - (Yellow LED) Indicates when IDE activity occurs. *Booting* - (Rightmost Red LED) Indicates BIOS Boot is in progress. When LED is off, CPU has finished POST. Once booting completes, any VME "SYSFAILS" is indicated by this LED.
RST	*Reset* - Allows the system to be reset from the front panel.
GbE Link/Active	Indicates the Ethernet is active, (Yellow LED).
GbE Speed	Indicates Link Speed. LED off indicates 10Base-T mode. Yellow LED indicates 100Base-TX, Green LED indicates 1000Base-T.
10/100 Link/Active	Indicates the Ethernet is active, (Yellow LED).
10/100 Speed	Indicates 10Base-T or 100Base-TX. Yellow LED indicates 10Base-T, Green LED indicates 100Base-TX.

In addition, the front-panel LEDs are used to indicate various modes of operational status that can occur with the VMIVME-7851/VME-7851RC. The table below is a summary of these indications.

Table 1-9 Status Indications

State	Indication
Board is in Reset	"10/100 Speed" LED rapidly alternates Yellow/Green and the Red "Reset" LED is illuminated.
VME SYSFAIL	Red "Booting" LED illuminates with each VME SYSFAIL 'seen' on the bus. The LED will remain on as long as the failure lasts.
Normal Operation	Reset LED Off (out of reset) Power LED On (power is good) Indicator LED Off, or Flashing (IDE activity) Booting LED Off (boot completed)

1.8 BIOS Setup

The VMIVME-7851/VME-7851RC have an onboard BIOS Setup program (AMI BIOS) that controls many configuration options. These options are saved in non-volatile, battery-backed memory and are collectively referred to as the board's "CMOS Configuration." The CMOS configuration controls many details concerning the behavior of the hardware from the moment power is applied.

The VMIVME-7851/VME-7851RC are shipped from the factory with hard drive type configuration set to AUTO in the CMOS.

1.9 Battery Mounted in Clip-Style Holder

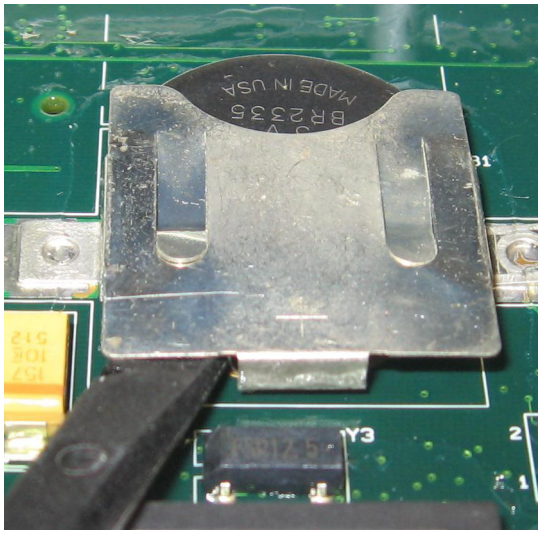
1.9.1 For Battery Removal:

1. Remove the board from the chassis and then separate the Main board and Expansion board. The battery is located on the Main board. If further help is needed locating the battery on the board, see **Figure 1-1**.
2. Remove the battery from the retaining clip by sliding it out of the clip, using a nonconductive tool.

1.9.2 For Battery Installation:

1. Use a Rayovac BR2335 3V coin battery for the replacement battery.
2. Observe correct polarity.
   Ensure the positive side of the battery, marked by a + sign, is facing up, away from the board.
3. Slide the new battery into the retaining clip.

Figure 1-4 Battery Removal/Installation



CAUTION

There is a risk of explosion if the battery is replaced with an incorrect type. Dispose of used batteries according to the manufacturer's instructions.

2 • Standard Features

The VMIVME-7851/VME-7851RC are Intel Pentium 4 Processor - M-based single board computers compatible with modern industry standard desktop systems. The VMIVME-7851/VME-7851RC therefore retain industry standard memory and I/O maps along with a standard interrupt architecture. The integrated peripherals described in this section (such as serial ports, USB ports, IDE drives, floppy drives, video controller, Ethernet controller and Ultra160 SCSI controllers) are all memory mapped the same as similarly equipped desktop systems, ensuring compatibility with modern operating systems.

The following sections describe the standard features of the VMIVME-7851/ VME-7851RC.

2.1 CPU Speed and RAM

The VMIVME-7851/VME-7851RC CPU sockets are factory populated with highspeed Pentium 4 Processor - M. The CPU speed and RAM/CompactFlash size are user specified as part of the VMIVME-7851/VME-7851RC ordering information.

To change CPU speeds, RAM size or CompactFlash size contact Customer Care to receive a Return Material Authorization (RMA).

GE Customer Care is available at:
1-800-433-2682, 1-780-401-7700.

Or, visit our website **www.ge-ip.com**

2.2 Physical Memory

The VMIVME-7851/VME-7851RC provide DDR Synchronous DRAM (SDRAM) as onboard system memory. Memory can be accessed as bytes, words or longwords.

The VMIVME-7851/VME-7851RC accept one PC1600 DDR SDRAM SODIMM for a maximum capacity of 1 GByte. The onboard SDRAM is dual-ported to the VME bus through the PCI-to-VME bridge and is addressable by the local processor, as well as the VME slave interface by another VME master. Caution must be used when sharing memory between the local processor and the VME to prevent a VME master from overwriting the local processor's operating system.

The VMIVME-7851/VME-7851RC include 32KB of non-volatile SRAM which can be accessed by the CPU at any time, and is used to store system data that must not be lost during power-off conditions.

NOTE

Memory capacity may be extended as parts become available.

2.3 Memory and Port Maps

Memory Map - Tundra Universe II-Based PCI-to-VME Bridge

The memory map for the Tundra Universe II-based interface for the VMIVME-7851/ VME-7851RC is shown in Table 2-1. All systems share this same memory map, although a VMIVME-7851/VME-7851RC with less than the full 256 MByte of SDRAM does not fill the entire space reserved for onboard Extended Memory.

Table 2-1 VMIVME-7851/VME-7851RC, Universe II-Based Interface Memory Address Map

MODE	MEMORY ADDRESS RANGE	SIZE	DESCRIPTION
PROTECTED MODE	$FFFF 0000 - $FFFF FFFF	64 KByte	ROM BIOS Image
	$0400 0000 - $FFFE FFFF	3.9 GByte	Unused *
	$0010 0000 - $0FFF FFFF	255 MByte	Reserved for Onboard Extended Memory (not filled on all systems)**
REAL MODE	$A0000 - $FFFFF	384 KByte	Reserved for BIOS Area
	$00000 - $9FFFF	640 KByte	Unused

* This space can be used to set up protected mode PCI-to-VME windows (also referred to as PCI slave images). BIOS will also map onboard PCI based NVRAM, Timers and Watchdog Timers in this area.
** This space can be allocated as shared memory (for example, between the Pentium processor-based CPU and VME Master). Note that if a PMC board is loaded, the expansion BIOS may be placed in this area.

2.4 I/O Port Map

Like a desktop system, the VMIVME-7851/VME-7851RC include special input/ output instructions that access I/O peripherals residing in I/O addressing space (separate and distinct from memory addressing space). Locations in I/O address space are referred to as ports. When the CPU decodes and executes an I/O instruction, it produces a 16-bit I/O address on lines A00 to A15 and identifies the I/O cycle with the M/I/O control line. Thus, the CPU includes an independent 64KB I/O address space, which is accessible as bytes, words or longwords.

Standard hardware circuitry reserves only 1,024 bytes of I/O addressing space from I/O $000 to $3FF for peripherals. All standard PC I/O peripherals, such as serial and parallel ports, hard and floppy drive controllers, video system, real-time clock, system timers and interrupt controllers are addressed in this region of I/O space. The BIOS initializes and configures all these registers properly; adjusting these I/O ports directly is not normally necessary.

The assigned and user-available I/O addresses are summarized in the I/O Address Map, Table 2-2.

Table 2-2 VMIVME-7851/VME-7851RC I/O Address Map

I/O ADDRESS RANGE	SIZE IN BYTES	HW DEVICE	PC/AT FUNCTION
$000 - $00F	16		DMA Controller 1 (Intel 8237A Compatible)
$010 - $01F	16		Reserved
$020 - $021	2		Master Interrupt Controller (Intel 8259A Compatible)
$022 - $03F	30		Reserved
$040 - $043	4		Programmable Timer (Intel 8254 Compatible)
$044 - $05F	30		Reserved
$060 - $064	5		Keyboard, Speaker, System Configuration (Intel 8042 Compatible)
$065 - $06F	11		Reserved
$070 - $071	2		Real-Time Clock
$072 - $07F	14		Reserved
$080 - $08F	16		DMA Page Registers
$090 - $091	2		Reserved
$092	1		Alt. Gate A20/Fast Reset Register
$093 - $09F	11		Reserved
$0A0 - $0A1	2		Slave Interrupt Controller (Intel 8259A Compatible)
$0A2 - $0BF	30		Reserved
$0C0 - $0DF	32		DMA Controller 2 (Intel 8237A Compatible)
$0E0 - $16F	142		Reserved
$170 - $177	8	ICH4-M	Secondary Hard Disk Controller
$178 - $1EF	120		User I/O
$1F0 - $1F7	8	ICH4-M	Primary Hard Disk Controller
$1F8 - $277	128		User I/O
$278 - $27F	8	I/O Chip*	LPT2 Parallel I/O
$280 - $2E7	104		Reserved
$2E8 - $2EE	7	UART*	COM4 Serial I/O*
$2EF - $2F7	9		User I/O
$2F8 - $2FE	7	Super-I/O Chip	COM2 Serial I/O (16550 Compatible)
$2FF - $36F	113		Reserved
$370 - $377	8	Super-I/O Chip	Secondary Floppy Disk Controller
$378 - $37F	8	Super-I/O Chip*	LPT1 Parallel I/O*
$380 - $3E7	108		Reserved
$3E8 - $3EE	7	UART*	COM3 Serial I/O*
$3F0 - $3F7	8	Super-I/O Chip	Primary Floppy Disk Controller
$3F8 - $3FE	7	Super-I/O Chip	COM1 Serial I/O (16550 Compatible)
$3FF - $4FF	256		Reserved
$500 - CFF	2048		Reserved

* While these I/O ports are reserved for the listed functions, they are not implemented on the VMIVME-7851/VME-7851RC. They are listed here to make the user aware of the standard PC usage of these ports.

2.5 Interrupts

2.5.1 System Interrupts

In addition to an I/O port address, an I/O device has a separate hardware interrupt line assignment. Assigned to each interrupt line is a corresponding interrupt vector in the 256-vector interrupt table at $00000 to $003FF in memory. The sixteen maskable interrupts and the single Non-Maskable Interrupt (NMI) are listed in Table 2-3 along with their functions. **Table 2-4 on page 36** details the vectors in the interrupt vector table. The interrupt number in HEX and decimal are also defined for real and protected mode in **Table 2-4 on page 36**.

The interrupt hardware implementation on the VMIVME-7851/VME-7851RC is standard for computers built around the PC architecture that evolved from the IBM PC/XT. In the IBM PC/XT computers, only eight interrupt request lines exist, numbered from IRQ0 to IRQ7 at the PIC. The IBM PC/AT computer added eight more IRQx lines, numbered IRQ8 to IRQ15, by cascading a second slave PIC into the original master PIC. IRQ2 at the master PIC was committed as the cascade input from the slave PIC. This architecture is represented in **Figure 2-1 on page 39**.

To maintain backward compatibility with PC/XT systems, IBM chose to use the new IRQ9 input on the slave PIC to operate as the old IRQ2 interrupt line on the PC/XT Expansion Bus. Thus, in AT systems, the IRQ9 interrupt line connects to the old IRQ2 pin (pin B4) on the AT Expansion Bus (or ISA bus).

Table 2-3 PC Hardware Interrupt Line Assignments

IRQ	AT FUNCTION	COMMENTS
NMI	Parity Errors (Must be enabled in BIOS Setup)	Used by VMIVME-7851/ VME-7851RC PCIbus Interface
0	System Timer	Set by BIOS Setup
1	Keyboard	Set by BIOS Setup
2	Duplexed to IRQ9	
3	COM2	
4	COM1	
5	Not Assigned	Determined by BIOS
6	Floppy Controller	
7	Parallel Port	
8	Real-Time Clock	
9	Not Assigned	Determined by BIOS
10	Not Assigned	Determined by BIOS
11	Not Assigned	Determined by BIOS
12	Mouse	
13	Math Coprocessor	
14	Primary IDE	Routed to P2 Only*
15	Secondary IDE	CF Type I/II, 1.8” or 2.5” drive*

*Determined by BIOS if no IDE devices are present

Table 2-4 PC Interrupt Vector Table

INTERRUPT NO.		IRQLINE	REAL MODE	PROTECTED MODE
HEX	DEC			
00	0		Divide Error	Same as Real Mode
01	1		Debug Single Step	Same as Real Mode
02	2	NMI	Memory Parity Error, VME Interrupts	Same as Real Mode (Must be enabled in BIOS Setup)
03	3		Debug Breakpoint	Same as Real Mode
04	4		ALU Overflow	Same as Real Mode
05	5		Print Screen	Array Bounds Check
06	6			Invalid OpCode
07	7			Device Not Available
08	8	IRQ0	Timer Tick	Double Exception Detected
09	9	IRQ1	Keyboard Input	Coprocessor Segment Overrun
0A	10	IRQ2	BIOS Reserved	Invalid Task State Segment
0B	11	IRQ3	COM2 Serial I/O	Segment Not Present
0C	12	IRQ4	COM1 Serial I/O	Stack Segment Overrun
0D	13	IRQ5	Unassigned	Unassigned
0E	14	IRQ6	Floppy Disk Controller	Page Fault
0F	15	IRQ7	Unassigned	Unassigned
10	16		BIOS Video I/O	Coprocessor Error
11	17		System Configuration Check	Same as Real Mode
12	18		Memory Size Check	Same as Real Mode
13	19		XT Floppy/Hard Drive	Same as Real Mode
14	20		BIOS Comm I/O	Same as Real Mode
15	21		BIOS Cassette Tape I/O	Same as Real Mode
16	22		BIOS Keyboard I/O	Same as Real Mode
17	23		BIOS Printer I/O	Same as Real Mode
18	24		ROM BASIC Entry Point	Same as Real Mode
19	25		Bootstrap Loader	Same as Real Mode
1A	26		Time of Day	Same as Real Mode
1B	27		Control/Break Handler	Same as Real Mode
1C	28		Timer Control	Same as Real Mode
1D	29		Video Parameter Table Pntr	Same as Real Mode
1E	30		Floppy Parm Table Pntr	Same as Real Mode
1F	31		Video Graphics Table Pntr	Same as Real Mode
20	32		DOS Terminate Program	Same as Real Mode
21	33		DOS Function Entry Point	Same as Real Mode
22	34		DOS Terminate Handler	Same as Real Mode
23	35		DOS Control/Break Handler	Same as Real Mode
24	36		DOS Critical Error Handler	Same as Real Mode
25	37		DOS Absolute Disk Read	Same as Real Mode
26	38		DOS Absolute Disk Write	Same as Real Mode
27	39		DOS Program Terminate, Stay Resident	Same as Real Mode
28	40		DOS Keyboard Idle Loop	Same as Real Mode
29	41		DOS CON Dev. Raw Output	Same as Real Mode

Table 2-4 PC Interrupt Vector Table (Continued)

INTERRUPT NO.		IRQLINE	REAL MODE	PROTECTED MODE
HEX	DEC			
2A	42		DOS 3.x+ Network Comm	Same as Real Mode
2B	43		DOS Internal Use	Same as Real Mode
2C	44		DOS Internal Use	Same as Real Mode
2D	45		DOS Internal Use	Same as Real Mode
2E	46		DOS Internal Use	Same as Real Mode
2F	47		DOS Print Spooler Driver	Same as Real Mode
30-60	48-96		Reserved by DOS	Same as Real Mode
61-66	97-102		User Available	Same as Real Mode
67-6F	103-111		Reserved by DOS	Same as Real Mode
70	112	IRQ8	Real Time Clock	
71	113	IRQ9	Redirect to IRQ2	
72	114	IRQ10	Not Assigned	
73	115	IRQ11	Not Assigned	
74	116	IRQ12	Mouse	
75	117	IRQ13	Math Coprocessor	
76	118	IRQ14	Primary IDE	
77	119	IRQ15	Secondary IDE	
78-7F	120-127		Reserved by DOS	Same as Real Mode
80-F0	128-240		Reserved for BASIC	Same as Real Mode
F1-FF	241-255		Reserved by DOS	Same as Real Mode

PCI Interrupts

Interrupts on Peripheral Component Interconnect (PCI) Local Bus are optional and defined as “level sensitive,” asserted low (negative true), using open drain output drivers. The assertion and de-assertion of an interrupt line, INTx#, is asynchronous to CLK. A device asserts its INTx# line when requesting attention from its device driver. Once the INTx# signal is asserted, it remains asserted until the device driver clears the pending request. When the request is cleared, the device de-asserts its INTx# signal.

PCI defines one interrupt line for a single function device and up to four interrupt lines for a multifunction device or connector. For a single function device, only INTA# may be used while the other three interrupt lines have no meaning. **Figure 2-1 on page 39** depicts the VMIVME-7851/VME-7851RC interrupt logic pertaining to VME operations and the PMC site.

Any function on a multifunction device can be connected to any of the INTx# lines. The Interrupt Pin register defines which INTx# line the function uses to request an interrupt. If a device implements a single INTx# line, it is called INTA#; if it implements two lines, they are called INTA# and INTB#; and so forth. For a multifunction device, all functions may use the same INTx# line, or each may have its own (up to a maximum of four functions), or any combination thereof. A single function can never generate an interrupt request on more than one INTx# line.

The slave PIC accepts the VME interrupts through lines that are defined by the BIOS. The BIOS defines which interrupt line to utilize depending on which system requires use of the line.

2.5.2 PCI Device Interrupt Map

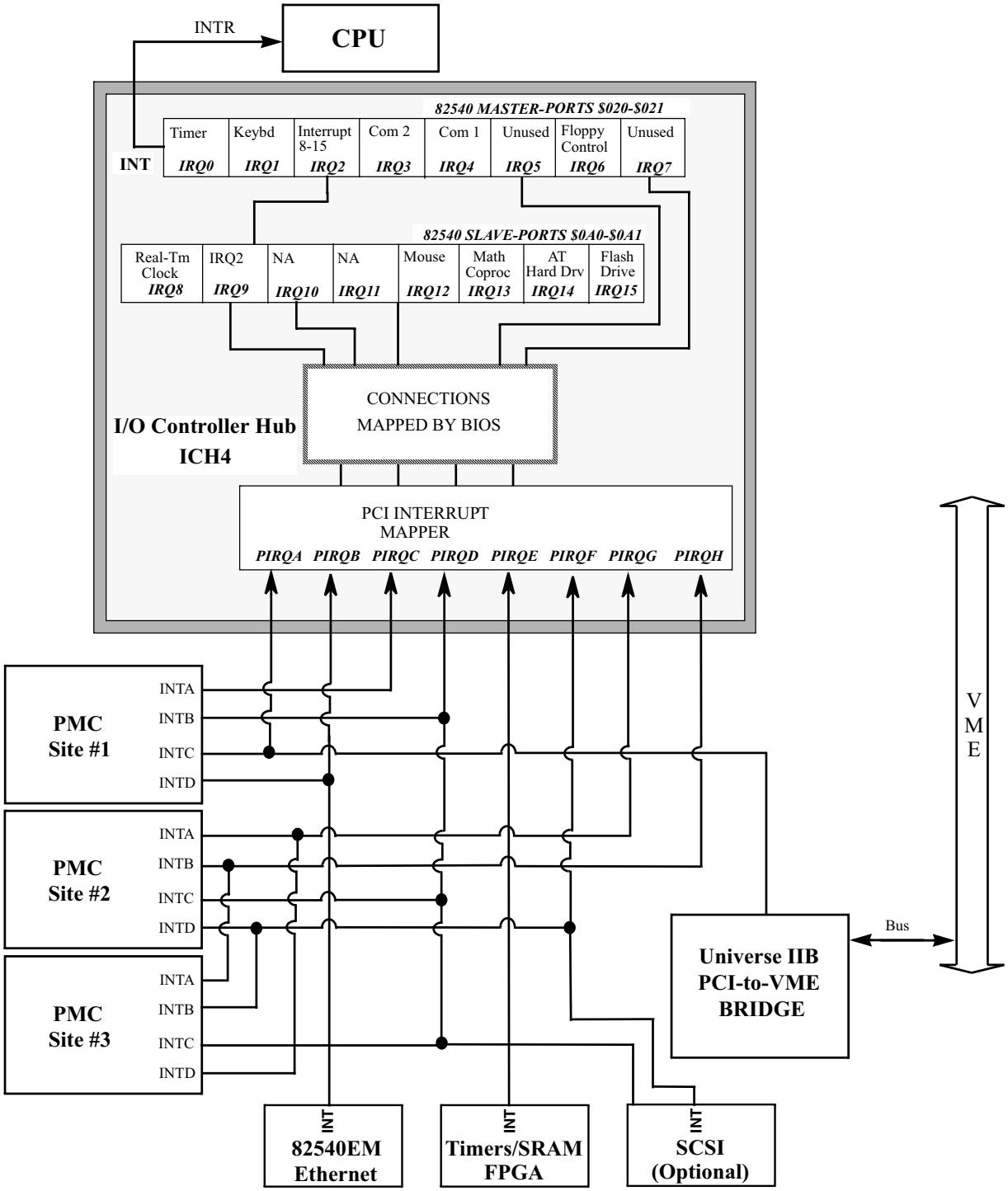
The PCI bus-based external devices include the PMC sites, Ethernet controller and the PCI-to-VME bridge. The default BIOS maps these external devices to the PCI Interrupt Request (PIRQx) lines of the ICH4. This mapping is illustrated in **Figure 2-1 on page 39** and is defined in Table 2-5.

The device PCI interrupt lines (INTA through INTD) that are present on each device cannot be modified.

Table 2-5 PCI Device Interrupt Mapping by the BIOS

DEVICE	COMPONENT	VENDOR ID	Device ID	CPU ADDRESS MAP ID SELECT	PCI IRQ	Arbitration Request Line
PCI-to-VME Bridge	Tundra Universe IIB	0x10E3	0x0000	AD19	INTA	REQ0
Timer/SRAM FPGA	GE Proprietary	0x114A	0x0004	AD20	INTE	N/A
PMC 1	N/A	N/A	N/A	AD31	INTC	REQ2
Gbit Ethernet Controller	Intel 82540EM or Intel 82541PI*	0x8086	0x100E 0x1076	AD22	INTB	REQ1
PCI Host Bridge	GMCH	0x8086	0x3580	N/A	N/A	N/A
Memory Controller	GMCH	0x8086	0x3584	N/A	N/A	N/A
Configuration and Process	GMCH	0x8086	0x3585	N/A	N/A	N/A
Integrated Graphics	GMCH	0x8086	0x3582	N/A	N/A	N/A
PCI-LPC Bridge	ICH4-M	0x8086	0x24CC	N/A	N/A	N/A
USB VHCI Controller	ICH4-M	0x8086	0x24C2	N/A	N/A	N/A
SMBus Controller	ICH4-M	0x8086	0x24C3	N/A	N/A	N/A
LAN Controller	ICH4-M	0x8086	0x10E3	N/A	N/A	N/A
USB VHCI Controller	ICH4-M	0x8086	0x24CD	N/A	N/A	N/A
PCI-to-Hub Bridge	ICH4-M	0x8086	0x2448	N/A	N/A	N/A
SCSI Controller A	LSI 53C1010	0x1000	0x0021	AD17	INTD	REQ3
SCSI Controller A	LSI 53C1010	0x1000	0x0021	AD17	INTF	REQ3
PMC 2	N/A	N/A	N/A	AD18	INTG	REQ4
PMC 3	N/A	N/A	N/A	AD21	INTH	REQ5

Figure 2-1 Connections for the PC Interrupt Logic Controller



The PCI-to-VME Bridge has the capability of generating an NMI via the PCI SERR# line. Table 2-6 describes the register bits that are used by the NMI. The SERR interrupt is routed through logic back to the NMI input line on the CPU. The CPU reads the NMI Status Control register to determine the NMI source (bits set to 1). After the NMI interrupt routine processes the interrupt, software clears the NMI status bits by setting the corresponding enable/disable bit to 1. The NMI Enable and Real-Time Clock register can mask the NMI signal and disable/enable all NMI sources.

Table 2-6 NMI Register Bit Descriptions

Status Control Register (I/O Address $061, Read/Write, Read Only)	
Bit 7	SERR# NMI Source Status (Read Only) - This bit is set to 1 if a system board agent detects a system board error. It then asserts the PCI SERR# line. To reset the interrupt, set Bit 2 to 0 and then set it to 1. When writing to port $061, Bit 7 must be 0.
Bit 2	PCI SERR# Enable (Read/Write) - 1 = Clear and Disable, 0 = Enable
Enable and Real-Time Clock Address Register (I/O Address $070, Write Only)	
Bit 7	NMI Enable - 1 = Disable, 0 = Enable

2.6 Integrated Peripherals

The VMIVME-7851/VME-7851RC incorporate two National Semiconductor Super I/O (SIO) chips. The primary SIO located on the main board provides the VMIVME-7851/VME-7851RC with a standard floppy drive controller, two 16550 UART-compatible serial ports, keyboard and mouse ports and general purpose I/O for system monitoring functions. Both serial port signals are available from the front panel. The floppy signals are available via the VME backplane connectors and can be accessed with the appropriate RTM (VMIACC-0562/ ACC-0562RC). A parallel port is provided via a second Super I/O chip located on the expansion board.

The IDE interface is provided by the Intel I/O Controller Hub (ICH4-M) chip. The IDE interface supports two channels known as the primary and secondary channels. The secondary channel is routed onboard to three CompactFlash sockets and either a 1.8" or 2.5" hard drive socket. The primary channel is routed out the VME backplane and can be accessed with the appropriate RTM (VMIACC-0562/ACC-0562RC) which terminates into a standard 40-pin header. Each channel can support two drives, a master and slave. Both IDE interfaces on the VMIVME-7851/VME-7851RC support Ultra ATA/33, Ultra ATA/66 and Ultra ATA/100 drives and automatically determine the proper operating mode based on the type of drive used. For drives connected to the VMIACC-0562/ACC-0562RC to properly function in the Ultra ATA/100 mode, a special 80 conductor cable must be used instead of the standard 40 conductor cable. This cable is typically available from the Ultra ATA/100 drive manufacturer.

NOTE

Although the VMIVME-7851/VME-7851RC has three CompactFlash sockets and a hard drive socket, these are all on the same secondary channel and therefore only two devices can reside on the bus at a time (one master and one slave).

2.7 Ethernet Controller

The network capability is provided by an external Ethernet Controller (the Intel 82540EM for the VMIVME-7851 or the Intel 82541PI for the VME-7851RC) and a MAC (Media Access Control) internal to the Intel ICH4 chip. The Ethernet controllers are PCI-based and are software configurable. The VMIVME-7851/ VME-7851RC support one 10Base-T and 100Base-TX Ethernet port (10/100) and one 10Base-T, 100Base-TX and 1000Base-T Ethernet port (GBE).

10Base-T A network based on the 10Base-T standard uses unshielded twisted-pair cables, providing an economical solution to networking by allowing the use of existing telephone wiring and connectors. The RJ45 connector is used with the 10Base-T standard. 10Base-T has a maximum length of 100 meters.

100Base-TX The VMIVME-7851/VME-7851RC also support the 100Base-TX Ethernet. A network based on a 100Base-TX standard uses unshielded twisted-pair cables and an RJ45 connector. 100Base-TX has a maximum length of 100 meters.

1000Base-T The VMIVME-7851/VME-7851RC support Gigabit Ethernet offering speeds of 1000Mb/s. It is fully compatible with existing Ethernets, as it uses the same CSMA/CD and MAC protocols. 1000Base-T has a maximum length of 3000 meters using Single-mode Fiber-Optic cables.

Boot ROM BIOS The VMIVME-7851/VME-7851RC support booting on the 10/100/1000 Mbit Ethernet port (GBE only) using a ROM Ethernet BIOS. Refer to Argon BIOS section for more information on remote Ethernet booting.

2.8 Video Graphics Adapter

High-resolution graphics and multimedia-quality video are supported on the VMIVME-7851/VME-7851RC using the 852GM (GMCH) chipset internal graphics controller. Screen resolutions up to 1,600 x 1,200 x 256 colors (single view mode) are supported by the graphics adapter.

Table 2-7 Supported Display Modes

	Bits Per Pixel (Frequency in Hz)		
Resolution	8-bit Indexed	16-bit	24-bit
320 x 200	70	70	70
320 x 240	70	70	70
352 x 480	70	70	70
352 x 576	70	70	70
400 x 300	70	70	70
512 x 384	70	70	70
640 x 400	70	70	70
640 x 480	60, 70, 72, 75, 85	60, 70, 72, 75, 85	60, 70, 72, 75, 85
720 x 480	75, 85	75, 85	75, 85
720 x 576	60, 75, 85	60, 75, 85	60, 75, 85
800 x 600	60, 70, 72, 75, 85	60, 70, 72, 75, 85	60, 70, 72, 75, 85
1,024 x 768	60, 70, 72, 75, 85	60, 70, 72, 75, 85	60, 70, 72, 75, 85
1,152 x 864	60, 70, 72, 75, 85	60, 70, 72, 75, 85	60, 70, 72, 75, 85
1,280 x 720	60, 75, 85	60, 75, 85	60, 75, 85
1,280 x 960	60, 75, 85	60, 75, 85	60, 75, 85
1,280 x 1,024	60, 70, 72, 75, 85	60, 70, 72, 75, 85	60, 70, 75, 85
1,600 x 900	60, 75, 85	60, 75, 85	
1,600 x 1,200	60, 70, 72, 75		

NOTE

Not all SVGA monitors support resolutions and refresh rates beyond 640 x 480 at 85Hz. Do not attempt to drive a monitor to a resolution or refresh rate beyond its capability.

2.8.1 Digital Visual Interface (DVI)

The VMIVME-7851/VME-7851RC have a Digital Visual Interface that provides a highspeed digital connection for visual data types that are display technology independent. DVI is a display interface developed in response to the proliferation of digital flat-panel displays. For the most part, these displays are currently connected to an analog Video Graphics Array (VGA) interface and, thus, require a double conversion.

The digital signal from the computer must be converted to an analog signal for the analog VGA interface, then converted back to a digital signal for processing by the flat-panel display. This inherently inefficient process takes a toll on performance and video quality and adds cost. In contrast, when a flat-panel display is connected to a digital interface, no digital-to-analog conversion is required.

DVI uses Silicon Image's PanelLink, a highspeed serial interface that uses Transition Minimized Differential Signaling (TMDS) to send data to the monitor. The DFP and VESA Plug and Display interfaces also use PanelLink. For this reason, DVI can work with these previous interfaces by using adapter cables (depending on the signal quality of the adapter.)

DVI also supports the VESA Display Data Channel (DDC) and the Extended Display Identification Data (EDID) specifications. DDC is a standard communications channel between the display adapter and monitor. EDID is a standard data format containing monitor information such as vendor information, monitor timing, maximum image size, and color characteristics. EDID information is stored in the display and is communicated over the DDC. EDID and DDC enable the system, display and graphics adapter to communicate so that the system can be configured to support specific features available in the display.

2.8.2 DVI Connectors

The DVI-I connector has 24 pins that can accommodate up to two TMDS links and the VESA DDC and EDID services. The DVI specification defines two types of connectors (see **Figure 1 on page 13**):

- DVI-Digital (DVI-D) supports digital displays only (not supported)
- DVI-Integrated (DVI-I) supports digital displays and is backward compatible with analog displays (used on the VMIVME-7851/VME-7851RC)

The VMIVME-7851/VME-7851RC use the DVI-I connector with a single TMDS link. The DVI-I interface accommodates a 12- or 24-pin DVI plug connector or a new type of analog plug connector that uses four additional pins, plus a ground plane plug to maintain a constant impedance for the analog RGB signals. The DVI-I adapter is supplied by GE.

2.9 Universal Serial Bus

The VMIVME-7851/VME-7851RC provide a single Universal Serial Bus (USB) connection on the front panel. The onboard USB controllers completely support the standard USB interface.

The USB Host Controller moves data between system memory and the USB by processing and scheduling data structures. The controller executes the scheduled lists, and reports status back to the system.

NOTE

Default CMOS settings of the VMIVME-7851/VME-7851RC have USB functions disabled. This allows more interrupts and less Interrupt Latency for Real Time system. If USB is enabled, the user must be aware that Interrupt Sharing and Latency will be affected.

3 • Embedded PC/RTOS Features

GE's VMIVME-7851/VME-7851RC feature additional capabilities beyond those of a typical desktop computer system. The units provide four software-controlled, general-purpose timers along with a programmable Watchdog Timer for synchronizing and controlling multiple events in embedded applications. The VMIVME-7851/VME-7851RC also provide a bootable CompactFlash system and 32 KByte of non-volatile SRAM. Also, the VMIVME-7851/VME-7851RC support an embedded intelligent VME bridge to allow compatibility with the most demanding VME applications. These features make the units ideal for embedded applications, particularly where standard hard drives and floppy disk drives cannot be used. The VMIVME-7851/VME-7851RC also support I^2C by integrating specialized circuitry for these functions.

3.1 VME Bus Bridge

In addition to its PC/AT functions, the VMIVME-7851/VME-7851RC have the following VME features:

- Complete six-line Address Modifier (AM-Code) programmability
- VME data interface with separate hardware byte/word swapping for master and slave accesses
- Support for VME64 multiplexed MBLT 64-bit VME block transfers
- User-configured interrupter
- User-configured interrupt handler
- System Controller mode with programmable VME arbiter (PRI, SGL and RRS modes are supported)
- VME BERR bus error timer (software programmable)
- Slave access from the VME to local RAM and mailbox registers
- Full-featured programmable VME requester (ROR, RWD and BCAP modes are supported)
- System Controller auto detection
- Complete VME master access through five separate Protected-mode memory windows

The VMIVME-7851/VME-7851RC support high-throughput DMA transfers of bytes, words and long-words in both Master and Slave configurations.

If Endian conversion is not needed, GE offers a special “Bypass” mode which can be used to further enhance throughput (not available for byte transfers).

The VMIVME-7851/VME-7851RC VME interface is provided by the PCI-to-VME bridge built around the Tundra Semiconductor Corporation Universe II VME interface chip. The Universe II provides a reliable high-performance 64-bit VME-to-PCI interface in one design. The functions and programming of the Universe-based VME interface are addressed in detail in a companion manual titled: *GE Tundra Universe II Based VMEbus Interface Product Manual (500-000211-000)*.

3.2 I²C Support

The VMIVME-7851/VME-7851RC support the I²C-bus and can operate as an I²C-bus master or slave per the I²C-bus specification, version 2.0, developed by Philips Semiconductor. Communication over the I²C-bus is accomplished through the use of the National Semiconductor Super I/O I²C-bus controller. This controller is capable of communicating on the I²C-bus on a byte-wise basis using interrupt or polled handshaking and supports a programmable clock rate when operating in Master mode. The I²C-bus signals are available through the VMIVME-7851/ VME-7851RC 's E12 header as shown in Table 3-1.

Table 3-1 I²C-bus Through E12

Signal Name	Pin
+5.0V	1
I²C_SDA	2
I²C_SCL	3
GND	4

The VMIVME-7851/VME-7851RC provide termination on the I²C signals.

The controller can issue interrupts to the VMIVME-7851/VME-7851RC when handshaking on the I²C-bus. When the I²C-bus controller drives the interrupt active, software must service and then clear the interrupt. Software can determine the cause of the interrupt by reading the bit of the status register.

For more information related to programming the I²C-bus controller, see the section "Access, Bus Interface (ACB)" in the "PC87366 128-pin LPC Super I/O with System Hardware Monitoring and MIDI and Game Ports" datasheet available from National Semiconductor.

3.3 Embedded PCI Functions

The VMIVME-7851/VME-7851RC provide non-volatile RAM (NVRAM), Timers and a Watchdog Timer via the PCI bus. These functions are required for embedded and real time applications. The PCI configuration space of these embedded functions are shown below.

Table 3-2 PCI Configuration Space Registers

31 16	15 00	Register Address
Device ID 0004	Vendor ID 114A	00h
Status	Command	04h
Class Code	Revision ID	08h
BIST / Header Type	Latency Timer / Cache Line Size	0Ch
PCI Base Address 0 for Memory-Mapped VME Control registers (BAR0)		10h
PCI Base Address 1 for Memory-Mapped 32kB NVRAM (BAR1)		14h
PCI Base Address 2 for memory-mapped Watchdog and other timers (BAR2)		18h
Reserved		1Ch
Reserved		20h
Reserved		24h
Reserved		28h
Subsystem ID 7851	Subsystem Vendor ID 114A	2Ch
Reserved		30h
Reserved		34h
Reserved		38h
Max_Lat / Min_gnt	Interrupt Pin / Interrupt Line	3Ch

The “Device ID” field indicates that the device is for VME products (00) and indicates the supported embedded feature set.

The “Vendor ID” and “Subsystem Vendor ID” fields indicate GE PICMG® assigned Vendor ID (114A).

The “Subsystem ID” field indicates the model number of the product (7851).

3.4 Timers

3.4.1 General

The VMIVME-7851/VME-7851RC provide four user-programmable timers (two 16-bit and two 32-bit) which are completely dedicated to user applications and are not required for any standard system function. Each timer is clocked by independent generators with selectable rates of 2 MHz, 1 MHz, 500 kHz and 250 kHz. Each timer may be independently enabled and each is capable of generating a system interrupt on timeout.

Events can be timed by either polling the timers or enabling the interrupt capability of the timer. A status register allows for application software to determine which timer is the cause of any interrupt.

3.4.2 Timer Control Status Register 1 (TCSR1)

The timers are controlled and monitored via the Timer Control Status Register 1 (TCSR1) located at offset 0x00 from the address in BAR2. The mapping of the bits in this register are as follows:

Table 3-3 Timer Control Status Register 1 (TCSR1)

Field	Bits	Read or Write
Timer 1 Caused IRQ	TCSR1[0]	R/W
Timer 1 Enable	TCSR1[1]	R/W
Timer 1 IRQ Enable	TCSR1[2]	R/W
Timer 1 Clock Select	TCSR1[4..3]	R/W
Timer 2 Caused IRQ	TCSR1[8]	R/W
Timer 2 Enable	TCSR1[9]	R/W
Timer 2 IRQ Enable	TCSR1[10]	R/W
Timer 2 Clock Select	TCSR1[12..11]	R/W
Timer 3 Caused IRQ	TCSR1[16]	R/W
Timer 3 Enable	TCSR1[17]	R/W
Timer 3 IRQ Enable	TCSR1[18]	R/W
Timer 3 Clock Select	TCSR1[20..19]	R/W
Timer 4 Caused IRQ	TCSR1[24]	R/W
Timer 4 Enable	TCSR1[25]	R/W
Timer 4 IRQ Enable	TCSR1[26]	R/W
Timer 4 Clock Select	TCSR1[28..27]	R/W
Reserved	All Other Bits	R/W
All of these bits default to "0" after system reset.		

Each timer has an independently selectable clock source which is selected by the bit pattern in the “Timer x Clock Select” field as follows:

Table 3-4 Timer x Clock Select

Clock Rate	MSb	LSb
2 MHz	0	0
1 MHz	0	1
500 kHz	1	0
250 kHz	1	1

Each timer can be independently enabled by writing a “1” to the appropriate “Timer x Enable” field. Similarly, the generation of interrupts by each timer can be independently enabled by writing a “1” to the appropriate “Timer x IRQ Enable” field.

If an interrupt is generated by a timer, the source of the interrupt may be determined by reading the “Timer x Caused IRQ” fields. If the field is set to “1”, then the respective timer caused the interrupt. Note that multiple timers can cause a single interrupt. Therefore, the status of all timers must be read to ensure that all interrupt sources are recognized.

A particular timer interrupt can be cleared by writing a “0” to the appropriate “Timer x Caused IRQ” field. Alternately, a write to the appropriate Timer x IRQ Clear (TxIC) register will also clear the interrupt. When clearing the interrupt using the “Timer x Caused IRQ” fields, note that it is important to ensure that a proper bit mask is used so that other register settings are not affected. The preferred method for clearing interrupts is to use the “Timer x IRQ Clear” registers described below.

3.4.3 Timer Control Status Register 2 (TCSR2)

The timers are also controlled by bits in the Timer Control Status Register 2 (TCSR2) located at offset 0x04 from the address in BAR2. The mapping of the bits in this register are as follows:

Table 3-5 Timer Control Status Register 2 (TCSR2)

Field	Bits	Read or Write
Read Latch Select	TCSR2[0]	R/W
Reserved	All Other Bits	R/W
All of these bits default to "0" after system reset.		

The "Read Latch Select" bit is used to select the latching mode of the programmable timers (see "Timers" section above). If this bit is set to "0", then each timer output is latched upon a read of any one of its address. For example, a read to the TMRCCR12 register latches the count of timers 1 and 2. A read to the TMRCCR3 register latches the count of timer 3. This continues for every read to any one of these registers. As a result, it is not possible to capture the values of all four timers at a given instance in time. However, by setting this bit to "1", all four timer outputs will be latched only on reads to the Timer 1 & 2 Current Count Register (TMRCCR12). Therefore, to capture the current count of all four timers at the same time, perform a read to the TMRCCR12 first (with a 32-bit read), followed by a read to TMRCCR3 and TMRCCR4. The first read (to the TMRCCR12 register) causes all four timer values to be latched at the same time. The subsequent reads to the TMRCCR3 and TMRCCR4 registers do not latch new count values, allowing the count of all timers at the same instance in time to be obtained.

3.4.4 Timer 1 & 2 Load Count Register (TMRLCR12)

Timers 1 & 2 are 16-bits wide and obtain their load count from the Timer 1 & 2 Load Count Register (TMRLCR12), located at offset 0x10 from the address in BAR2. The mapping of bits in this register are as follows:

Table 3-6 Timer 1 & 2 Load Count Register (TMRLCR12)

Field	Bits	Read or Write
Timer 2 Load Count	TMRLCR12[31..16]	R/W
Timer 1 Load Count	TMRLCR12[15..0]	R/W

When either of these fields are written (either by a single 32-bit write or separate 16-bit writes), the respective timer is loaded with the written value on the next rising edge of the timer clock, regardless of whether the timer is enabled or disabled. The value stored in this register is also automatically reloaded on terminal count (or timeout) of the timer.

3.4.5 Timer 3 Load Count Register (TMRLCR3)

Timer 3 is 32-bits wide and obtains its load count from the Timer 3 Load Count Register (TMRLCR3), located at offset 0x14 from the address in BAR2. The mapping of bits in this register are as follows:

Table 3-7 Timer 3 Load Count Register (TMRLCR3)

Field	Bits	Read or Write
Timer 3 Load Count	TMRLCR3[31..0]	R/W

When this field is written, Timer 3 is loaded with the written value on the next rising edge of the timer clock, regardless of whether the timer is enabled or disabled. The value stored in this register is also automatically reloaded on terminal count (or timeout) of the timer.

3.4.6 Timer 4 Load Count Register (TMRLCR4)

Timer 4 is 32-bits wide and obtains its load count from the Timer 4 Load Count Register (TMRLCR4), located at offset 0x18 from the address in BAR2. The mapping of bits in this register are as follows:

Table 3-8 Timer 4 Load Count Register (TMRLCR4)

Field	Bits	Read or Write
Timer 4 Load Count	TMRLCR4[31..0]	R/W

When this field is written, Timer 4 is loaded with the written value on the next rising edge of the timer clock, regardless of whether the timer is enabled or disabled. The value stored in this register is also automatically reloaded on terminal count (or timeout) of the timer.

3.4.7 Timer 1 & 2 Current Count Register (TMRCCR12)

The current count of timers 1 & 2 may be read via the Timer 1 & 2 Current Count Register (TMRCCR12), located at offset 0x20 from the address in BAR2. The mapping of bits in this register are as follows:

Table 3-9 Timer 1 & 2 Current Count Register (TMRCCR12)

Field	Bits	Read or Write
Timer 2 Count	TMRCCR12[31..16]	R.O.
Timer 1 Count	TMRCCR12[15..0]	R.O.

When either field is read, the current count value is latched and returned. There are two modes that determine how the count is latched depending on the setting of the “Read Latch Select” bit in the WDT Control Status Register (CSR2). See the CSR2 register description for more information on these two modes.

3.4.8 Timer 3 Current Count Register (TMRCCR3)

The current count of Timer 3 may be read via the Timer 3 Current Count Register (TMRCCR3), located at offset 0x24 from the address in BAR2. The mapping of bits in this register are as follows:

Table 3-10 Timer 3 Current Count Register (TMRCCR3)

Field	Bits	Read or Write
Timer 3 Count	TMRCCR3[31..0]	R.O.

When this field is read, the current count value is latched and returned. There are two modes that determine how the count is latched depending on the setting of the "Read Latch Select" bit in the WDT Control Status Register (CSR2). See the CSR2 register description for more information on these two modes.

3.4.9 Timer 4 Current Count Register (TMRCCR4)

The current count of Timer 4 may be read via the Timer 4 Current Count Register (TMRCCR4), located at offset 0x28 from the address in BAR2. The mapping of bits in this register are as follows:

Table 3-11 Timer 4 Current Count Register (TMRCCR4)

Field	Bits	Read or Write
Timer 4 Count	TMRCCR4[31..0]	R.O.

When this field is read, the current count value is latched and returned. There are two modes that determine how the count is latched depending on the setting of the "Read Latch Select" bit in the WDT Control Status Register (CSR2). See the CSR2 register description for more information on these two modes.

3.4.10 Timer 1 IRQ Clear (T1IC)

The Timer 1 IRQ Clear (T1IC) register is used to clear an interrupt caused by Timer 1. Writing to this register, located at offset 0x30 from the address in BAR2, causes the interrupt from Timer 1 to be cleared. This can also be done by writing a "0" to the appropriate "Timer x Caused IRQ" field of the timer Control Status Register (CSR1). This register is write only and the data written is irrelevant.

3.4.11 Timer 2 IRQ Clear (T2IC)

The Timer 2 IRQ Clear (T2IC) register is used to clear an interrupt caused by Timer 2. Writing to this register, located at offset 0x34 from the address in BAR2, causes the interrupt from Timer 2 to be cleared. This can also be done by writing a "0" to the appropriate "Timer x Caused IRQ" field of the timer Control Status Register (CSR1). This register is write only and the data written is irrelevant.

3.4.12 Timer 3 IRQ Clear (T3IC)

The Timer 3 IRQ Clear (T3IC) register is used to clear an interrupt caused by Timer 3. Writing to this register, located at offset 0x38 from the address in BAR2, causes the interrupt from Timer 3 to be cleared. This can also be done by writing a "0" to the appropriate "Timer x Caused IRQ" field of the timer Control Status Register (CSR1). This register is write only and the data written is irrelevant.

3.4.13 Timer 4 IRQ Clear (T4IC)

The Timer 4 IRQ Clear (T4IC) register is used to clear an interrupt caused by Timer 4. Writing to this register, located at offset 0x3C from the address in BAR2, causes the interrupt from Timer 4 to be cleared. This can also be done by writing a "0" to the appropriate "Timer x Caused IRQ" field of the timer Control Status Register (CSR1). This register is write only and the data written is irrelevant.

3.5 Watchdog Timer

The VMIVME-7851/VME-7851RC provide a programmable Watchdog Timer (WDT) which can be used to reset the system if software integrity fails.

3.5.1 WDT Control Status Register (WCSR)

The WDT is controlled and monitored by the WDT Control Status Register (WCSR) which is located at offset 0x08 from the address in BAR2. The mapping of the bits in this register are as follows:

Table 3-12 WDT Control Status Register (WCSR)

Field	Bits	Read or Write
SERR/RST Select	WCSR[16]	R/W
WDT Timeout Select	WCSR[10..8]	R/W
WDT Enable	WCSR[0]	R/W
All of these bits default to "0" after system reset. All other bits are reserved.		

The “WDT Timeout Select” field is used to select the timeout value of the Watchdog Timer as follows:

Table 3-13 WDT Timeout Select

Timeout	WCSR[10]	WCSR[9]	WCSR[8]
135s	0	0	0
33.6s	0	0	1
2.1s	0	1	0
524ms	0	1	1
262ms	1	0	0
131ms	1	0	1
32.768ms	1	1	0
2.048ms	1	1	1

The “SERR/RST Select” bit is used to select whether the WDT generates an SERR# on the local PCI bus or a system reset. If this bit is set to “0”, the WDT will generate a system reset. Otherwise, the WDT will make the local PCI bus SERR# signal active.

The “WDT Enable” bit is used to enable the Watchdog Timer function. This bit must be set to “1” in order for the Watchdog Timer to function. Note that since all registers default to zero after reset, the Watchdog Timer is always disabled after a reset. The Watchdog Timer must be re-enabled by the application software after reset in order for the Watchdog Timer to continue to operate. Once the Watchdog Timer is enabled, the application software must refresh the Watchdog Timer within the selected timeout period to prevent a reset or SERR# from being generated. The Watchdog Timer is refreshed by performing a write to the WDT Keepalive register (WKPA). The data written is irrelevant.

3.5.2 WDT Keepalive Register (WKPA)

When enabled, the Watchdog Timer is prevented from resetting the system by writing to the WDT Keepalive Register (WKPA) located at offset 0x0C from the address in BAR2 within the selected timeout period. The data written to this location is irrelevant.

3.5.3 NVSRAM

The VMIVME-7851/VME-7851RC provide 32KB of non-volatile SRAM. This memory is mapped in 32KB of address space starting at the address in BAR1. This memory is available at any time and supports byte, short word and long word accesses from the PCI bus. The contents of this memory is retained when the power to the board is removed.

3.5.4 VME Control

The following table shows the register definitions for the VMIVME-7851/ VME-7851RC (offset from BAR0).

Table 3-14 Register Definitions Offset From BAR0

Register Name	Offset	
VMECOMM	0x00	
Bit Name	Bit	Definition
MEC_SEL	0	Master big-endian enable bit 1=Big Endian 0=Little Endian bit
SEC_SEL	1	Slave Big-Endian enable bit 1=Big Endian 0=Little Endian
ABLE	2	Auxiliary BERR logic enable bit 1=Aux. BERR enabled 0=Aux. BERR disabled
BTO	3	Bus error timer enabled 1=enabled 0=disabled
BTOV [1:0]	5:4	Timeout value 00 - 16µS 01 - 64µS 10 -256µS 11 - 1.00mS
BERRI	6	BERR interrupt enable 1=Interrupt enabled 0=Interrupt disabled
BERRST	7	BERR status read/clear bit 1=Clear BERR status 0=Do nothing
SFENA	8	Enables generation of VME SYSFAIL upon WDT timeout 1= enable SYSFAIL generation 0=disable
Unused	9	Not Used
BPENA	10	Endian conversion bypass bit 1=Bypass 0=Not bypassed
VBENA	11	VME enable bit 1= enabled 0=disabled
Unused	31:12	Not Used
VBAR	0x04	
VME_ADDR	All	Latched VME Address
VBAM	0x08	
VME_ADDR	5:0	Latched VME Address Modifier
Unused	31:6	Not Used
SEC_SEL	0x001	

Please refer to Table 3-2, **PCI Configuration Space Registers** on page 48 for more information concerning BAR0.

3.6 Remote Ethernet Booting

The VMIVME-7851/VME-7851RC are capable of booting from a server over a network utilizing the Argon BIOS. The Argon BIOS gives you the ability to remotely boot the VMIVME-7851/VME-7851RC using a variety of network protocols. The Ethernet must be connected through the front panel (RJ45) connector to boot remotely. This feature allows users to create systems without the worry of disk drive reliability, or the extra cost of adding Flash drives.

NOTE

Remote Ethernet booting is only available from the 10/100/1000Base-T Ethernet port (GBE).

3.6.1 BootWare Features

- Netware (802.1, 802.3 or EthII), TCP/IP (DHCP or BootP), RPL and PXE boot support
- Unparalleled boot sector virus protection
- Detailed boot configuration screens
- Comprehensive diagnostics
- Optional disabling of local boots
- Dual-boot option lets users select network or local booting

4 • Optional Features

The VMIVME-7851/VME-7851RC feature optional capabilities beyond those of a typical IBM PC/AT-compatible CPU. Please contact Sales for details on ordering options. An optional dual Ultra160 SCSI interface is available. This feature makes the unit ideal for embedded applications, particularly applications where standard hard drives and floppy disk drives cannot be used.

4.1 Dual Ultra160 SCSI (Optional)

The VMIVME-7851/VME-7851RC optional Dual-Channel Ultra160 SCSI Host Adapter incorporates the LSI Logic SYM53C1010, a highly integrated PCI Dual-Channel Ultra160 SCSI controller. The SYM53C1010 is 100 percent compatible with the Ultra160 SCSI initiative and provides additional features that ensure robust Ultra160 system operation. Fast SCSI, Ultra SCSI, Ultra2 SCSI and Ultra160 SCSI are all supported by the SYM53C1010. Double transition clocking enables throughput of up to 160 MByte on each channel for a total of 320 MByte, without increasing the interface clock rate.

The SYM53C1010 uses the same CRC algorithm used by FDDI, Ethernet and Fibre Channel, and detects single bit errors, double bit errors, odd number of errors, and all burst errors up to 32 bits long. To provide complete end-to-end protection of the SCSI I/O, AIP protects all non-data phases, augmenting the CRC feature of Ultra160. SureLINK domain validation technology detects the configuration of the SCSI bus and automatically tests and adjusts the SCSI transfer rate to optimize inter-operability. The SYM53C1010 controller and Ultra160 provide Basic (Level 1) and Enhanced (Level 2) domain validation, while the SYM53C1010 has an added feature of Margining (Level 3) domain validation.

4.1.1 PCI Interface

The Ultra160 SCSI PCI Interface complies with PCI Local Bus Specification Revision 2.2, and implements a 32-bit/33 MHz PCI bus. The SYM53C1010 is a true PCI multi-function device in that it presents one electrical load to the PCI bus. It uses one REQ/-GNT/pair to arbitrate for PCI bus mastership, and separate interrupt signals are generated for SCSI Function A and SCSI Function B for maximum performance. The SYM53C1010 complies with PCI Power Management Interface Specification Revision 1.1 and PC 99, supporting power states D0, D1, D2, D3hot and D3cold, power management capabilities registers, and programmable values for PCI Subsystem Vendor ID and Subsystem ID. Extended access cycles (Memory Read Line, Memory Read Multiple, and Memory Write and Invalidate) are also supported.

4.1.2 Ultra160 SCSI Memory

The SYM53C1010 expansion ROM is located within the system BIOS. A serial 2-wire interface on each SCSI channel provides a connection to an external serial EEPROM for storing the Subsystem Vendor ID and Subsystem ID.

4.1.3 Ultra160 SCSI Processor

The SYM53C1010 provides two independent Ultra160 SCSI controllers on a single chip. Each controller supports wide Ultra160 SCSI synchronous transfer rates up to 160 MByte on an LVD SCSI bus. Integrated LVDlink transceivers support both LVD and single-ended signals with no external transceivers required. Fast SCSI, Ultra SCSI, Ultra2 SCSI and Ultra160 SCSI are all supported by the SYM53C1010. An onchip SCSI clock quadrupler allows the chip to achieve Ultra160 SCSI transfer rates with an input frequency of 40 MHz. The 8KB of internal RAM per channel for SCRIPTS instruction storage allow all accesses to remain internal, reducing the time spent on the PCI bus. A 944-byte DMA FIFO on each channel allows the device to efficiently burst up to 512 bytes across the PCI bus. SCSI bus phase mismatches are handled in SCRIPTS, reducing CPU utilization.

4.1.4 Ultra160 SCSI Termination

All SCSI buses require a termination network at each end to function properly. Specific termination requirements differ, depending on which types of SCSI devices are present on the bus. The SCSI Host Adapter uses the UCC5630A termination ICs to automatically sense the SCSI bus and switch the termination to either single ended (SE) or low voltage differential (LVD) SCSI, dependent on which type of devices are connected to the bus. The UCC5630A termination IC is used in multi-mode active termination applications, where SE and LVD devices might coexist. The UCC5630A has both SE and LVD termination networks integrated into a single monolithic component. The correct network is automatically determined by the SCSI bus “DIFSENS” signal. The SCSI bus DIFSENS signal line is used to identify which types of SCSI devices are present on the bus. On power-up, the UCC5630A DIFSENS drivers will attempt to deliver 1.3V to the DIFSENS line.

If only LVD devices are present, the DIFSENS line will be successfully driven to 1.3V and the terminators will configure for LVD operation. If any single ended devices are present, they will present a short to ground on the DIFSENS line, signaling the UCC5630A(s) to configure into the SE mode, accommodating the SE devices. Or, if any high voltage differential (HVD) devices are present, the DIFSENS line is pulled high and the terminator will enter a high impedance state, effectively disconnecting from the bus.

4.1.5 Media Connection

The VMIVME-7851/VME-7851RC support dual 68-pin VHDCI external connectors via J5 of the I/O expansion board.

In addition to being routed through the front panel connector (J5) differentially, SCSI Channel A is also routed as single-ended through the rear P2 connector. If the VMIACC-0561 SCSI transition panel is used, the entire Channel A becomes single-ended. Channel B can remain differential. If channel A has at least one device connected to J5, and another connected to the VMIACC-0561, then the VMIVME-7851/VME-7851RC ’s SYM53C1010 is essentially in the middle of the SCSI chain and should have its termination network disabled. This is accomplished by removing the jumper from E7.

Maintenance

If a GE product malfunctions, please verify the following:

1. Software version resident on the product
2. System configuration
3. Electrical connections
4. Jumper or configuration options
5. Boards are fully inserted into their proper connector location
6. Connector pins are clean and free from contamination
7. No components or adjacent boards were disturbed when inserting or removing the board from the chassis
8. Quality of cables and I/O connections

If products must be returned, contact GE for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return from Customer Care.**

GE Customer Care is available at: 1-800-433-2682 in North America, or +1-780-401-7700 for international calls. Or, visit our website **www.ge-ip.com.**

Maintenance Prints

User level repairs are not recommended. The drawings and diagrams in this manual are for reference purposes only.

Compliance Information

GE's VMIVME-7851/VME-7851RC have been evaluated to and met the requirements for compliance to the following standards:

International Compliance

- EN55022:1998/CISPR 22:1997
- IEC61000-4-2
- IEC61000-4-3
- IEC61000-4-4
- IEC61000-4-5
- IEC61000-4-6
- IEC61000-4-8

European Union (CE Mark)

- BS EN55024 (1998 w A1:01 & A2: 03)
- BS EN55022 (Class A)

United States

- FCC Part 15, Subpart B, Section 109, Class A

Australia/New Zealand

- AS/NZS CISPR 22 (2002) Class A

Canada

- ICES-003 Class A

FCC Part 15

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

FCC Class A

NOTE

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

CAUTION

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Canadian Regulations

The VMIVME-7851/VME-7851RC Class A digital apparatus complies with Canadian ICES-003.

NOTE

Any equipment tested and found compliant with FCC Part 15 for unintentional radiators or EN55022 (previously CISPR 22) satisfy ICES-003.

A • Appendix A: Connector Pinouts

The VMIVME-7851/VME-7851RC VME SBCs have several connectors for their I/O ports. Wherever possible, the VMIVME-7851/VME-7851RC use connectors and pinouts typical for any desktop PC. This ensures maximum compatibility with a variety of systems.

Connector diagrams in this appendix are generally shown in a natural orientation with the controller board mounted in a VME chassis.

A.1 VME Connector and Pinout (P1 and P2)

Figure A-1 on page 64 shows the location of the VME P1 and P2 connectors and their orientation on the VMIVME-7851/VME-7851RC.

Table A-1 on page 64 shows the pin assignments for the VME connectors on the main board. **Table A-2** on page 65 shows the pin assignments for the VME connectors on the expansion board.

NOTE

Only Row B of connector P2 should be bussed across the backplane; all other pins on P2 are reserved for GE transition cards (VMIACC-0561 and VMIACC-0562/ACC-0562RC).

Figure A-1 VME Connectors (P1/P2)

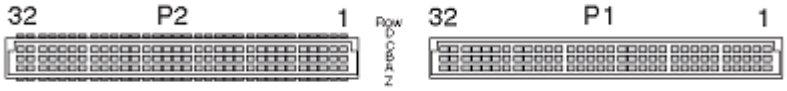


Table A-1 VME Connector Pinout Main Board

PIN #	P1 ROW A SIGNAL	P1 ROW B SIGNAL	P1 ROW C SIGNAL	P2 ROW Z SIGNAL	P2 ROW A SIGNAL	P2 ROW B SIGNAL	P2 ROW C SIGNAL	P2 ROW D SIGNAL
1	D00	BBSY#	D08	CONN [2]	CBL_DETECT	+5V	IDE RST#	CONN [1]
2	D01	BCLR#	D09	GND	DDP8	GND	DDP7	CONN [3]
3	D02	ACFAIL#	D10	CONN [5]	DDP9	NC	DDP6	CONN [4]
4	D03	BG0IN#	D11	GND	DDP10	A24	DDP5	CONN [6]
5	D04	BG0OUT#	D12	CONN [8]	DDP11	A25	DDP4	CONN [7]
6	D05	BG1IN#	D13	GND	DDP12	A26	DDP3	CONN [9]
7	D06	BG1OUT#	D14	CONN [11]	DDP13	A27	DDP2	CONN [10]
8	D07	BG2IN#	D15	GND	DDP14	A28	DDP1	CONN [12]
9	GND	BG2OUT#	GND	CONN [14]	DDP15	A29	DDP0	CONN [13]
10	SYSCLK	BG3IN#	SYSFAIL#	GND	IDE REQ	A30	1k pull-up +5V	CONN [15]
11	GND	BG3OUT#	BERR#	CONN [17]	IDE IOW#	A31	GND	CONN [16]
12	DS1#	BR0#	SYSRESET#	GND	IDE IOR#	GND	GND	CONN [18]
13	DS0#	BR1#	LWORD#	CONN [20]	IDE IORDY#	+5V	GND	CONN [19]
14	WRITE#	BR2#	AM5	GND	GND	D16	470 Ohm pull-down	CONN [21]
15	GND	BR3#	A23	CONN [23]	GND	D17	IDE DACK0#	CONN [22]
16	DTACK#	AM0	A22	GND	GND	D18	IDE IRQ14	CONN [24]
17	GND	AM1	A21	CONN [26]	DAP1	D19	DAP 2	CONN [25]
18	AS#	AM2	A20	GND	IDECS1#	D20	DAP 0	CONN [27]
19	GND	AM3	A19	CONN [29]	HD_ACT#	D21	IDE CS3#	CONN [28]
20	IACK#	GND	A18	GND	DRATE0	D22	DENSEL	CONN [30]
21	IACKIN#	NC	A17	CONN [32]	GND	D23	INDEX#	CONN [31]
22	IACKOUT#	NC	A16	GND	DRVSB #	GND	MOTEA#	CONN [33]
23	AM4	GND	A15	CONN [35]	GND	D24	DRVSA#	CONN [34]
24	A07	IRQ7#	A14	GND	GND	D25	MOTEB#	CONN [36]
25	A06	IRQ6#	A13	CONN [38]	GND	D26	STEP#	CONN [37]
26	A05	IRQ5#	A12	GND	GND	D27	WDATA#	CONN [39]
27	A04	IRQ4#	A11	CONN [41]	GND	D28	TRK#	CONN [40]
28	A03	IRQ3#	A10	GND	GND	D29	RDATA#	CONN [42]
29	A02	IRQ2#	A09	CONN [44]	DSKCHG #	D30	SIDE1#	CONN [43]
30	A01	IRQ1#	A08	GND	GND	D31	DIR#	CONN [45]
31	-12V	NC	+12V	CONN [46]	+5V	GND	WGATE#	GND
32	+5V	+5V	+5V	GND	+5V	+5V	WPT#	NC

Table A-2 VME Connector Pinout PMC#2 I/O and SCSI (Expansion Board)

PIN #	P1 ROW A SIGNAL	P1 ROW B SIGNAL	P1 ROW C SIGNAL	P2 ROW Z SIGNAL	P2 ROW A SIGNAL	P2 ROW B SIGNAL	P2 ROW C SIGNAL	P2 ROW D SIGNAL
1	NC	NC	NC	CONN [2]	A_SD[12]-	+5V	CONN [53]	CONN [1]
2	NC	NC	NC	GND	GND	GND	A_SD [13]-	CONN [3]
3	NC	NC	NC	CONN [5]	A_SD[14]-	NC	A_DIFFSEN	CONN [4]
4	NC	BG0	NC	GND	GND	NC	A_SD [15]-	CONN [6]
5	NC	BG0	NC	CONN [8]	A_SDP1-	NC	GND	CONN [7]
6	NC	BG1	NC	GND	A_SD[0]-	NC	A_SD [1]-	CONN [9]
7	NC	BG1	NC	CONN [11]	GND	NC	GND	CONN [10]
8	NC	BG2	NC	GND	A_SD[2]-	NC	A_SD [3]-	CONN [12]
9	GND	BG2	GND	CONN [14]	GND	NC	GND	CONN [13]
10	NC	BG3	NC	GND	A_SD [4]-	NC	A_SD [5]-	CONN [15]
11	GND	BG3	NC	CONN [17]	GND	NC	GND	CONN [16]
12	NC	NC	NC	GND	A_SD [6]-	GND	A_SD [7]-	CONN [18]
13	NC	NC	NC	CONN [20]	CONN [54]	+5V	CONN [56]	CONN [19]
14	NC	NC	NC	GND	A_SDP0-	NC	A_SATN-	CONN [21]
15	GND	NC	NC	CONN [23]	GND	NC	GND	CONN [22]
16	NC	NC	NC	GND	A_SBSY-	NC	A_SACK-	CONN [24]
17	GND	NC	NC	CONN [26]	GND	NC	GND	CONN [25]
18	NC	NC	NC	GND	A_SRST-	NC	A_SMSG-	CONN [27]
19	GND	NC	NC	CONN [29]	GND	NC	GND	CONN [28]
20	NC	GND	NC	GND	A_SSEL-	NC	A_SC_D-	CONN [30]
21	IACK	NC	NC	CONN [32]	GND	NC	GND	CONN [31]
22	IACK	NC	NC	GND	A_SREQ-	GND	A_SI_0-	CONN [33]
23	NC	GND	NC	CONN [35]	GND	NC	GND	CONN [34]
24	NC	NC	NC	GND	CONN [50]	NC	A_TERMPWR_EX	CONN [36]
25	NC	NC	NC	CONN [38]	CONN [52]	NC	CONN [51]	CONN [37]
26	NC	NC	NC	GND	GND	NC	A_SD [9]-	CONN [39]
27	NC	NC	NC	CONN [41]	A_SD [8]-	NC	GND	CONN [40]
28	NC	NC	NC	GND	GND	NC	A_SD [11]-	CONN [42]
29	NC	NC	NC	CONN [44]	A_SD [10]-	NC	CONN [58]	CONN [43]
30	NC	NC	NC	GND	CONN [62]	NC	CONN [60]	CONN [45]
31	-12V	NC	+12V	CONN [46]	CONN [64]	GND	CONN [61]	CONN [47]
32	+5V	+5V	+5V	GND	+5V	+5V	CONN [63]	CONN [48]

A.2 Serial Connector Pinout

Each standard RS232 serial port connector is a Micro-DB9 male as shown in Figure A-2. Adapters to connect standard DB9 serial peripherals to the board are available and sold separately (GE P/N 360-010050-001 for the VMIVME-7851 or 360-93010050-001 for the VME-7851RC).

Figure A-2 Serial Connector GE

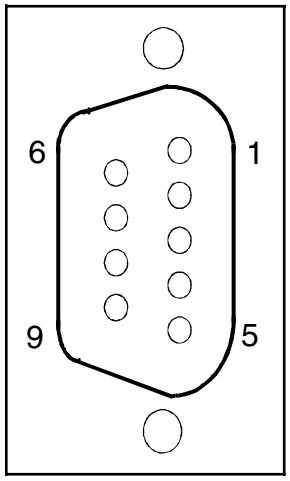


Table A-3 Serial Port Connectors COM1 and COM2

DB9 PIN	DIR	RS232 SIGNAL	FUNCTION
1	In	DCD	Data Carrier Detect
2	In	RX	Receive Data
3	Out	TX	Transmit Data
4	Out	DTR	Data Terminal Ready
5		GND	Signal Ground
6	In	DSR	Data Set Ready
7	Out	RTS	Request to Send
8	In	CTS	Clear to Send
9	In	RI	Ring Indicator
Shield			Chassis Ground

A.3 USB Connector

The USB port uses an industry standard single 4-position shielded connector. Figure A-3 shows the pinout of the USB connector.

Figure A-3 USB Connector

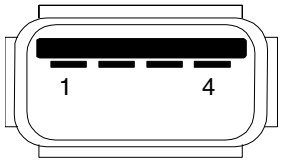


Table A-4 USB Connector Pinout

PIN	SIGNAL	FUNCTION
1	USBV	USB Power
2	USB-	USB Data -
3	USB+	USB Data +
4	USBG	USB Ground

A.4 Ethernet Connector Pinout (J4 and J5)

The pinout diagram for the Ethernet connectors is shown in Figure A-4.

Figure A-4 Ethernet Connector

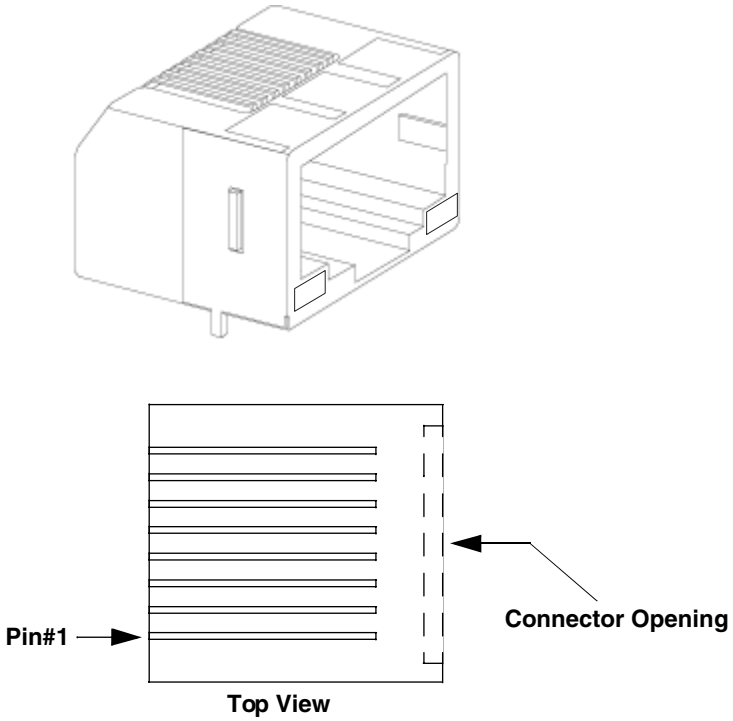


Table A-5 Ethernet Connector

PIN	Signal Name	Function
1	TD+	Transmit Data
2	TD-	Transmit Data
3	RD+	Receive Data
4	TX_CT_OUT	Transmit Center Tap Out
5	TX_CT_OUT	Transmit Center Tap Out
6	RD-	Receive Data
7	RX_CT_OUT	Receive Center Tap Out
8	RX_CT_OUT	Receive Center Tap Out

A.5 DVI-I Connector and Pinout (J10)

The DVI interface accommodates a 24-pin DVI-I connector that uses four additional pins, plus a ground plane plug to maintain a constant impedance for the analog RGB signals. The DVI-I adapter is included with the VMIVME-7851/ VME-7851RC.

Figure A-5 DVI-I Connector and DVI-I-to-SVGA Adapter

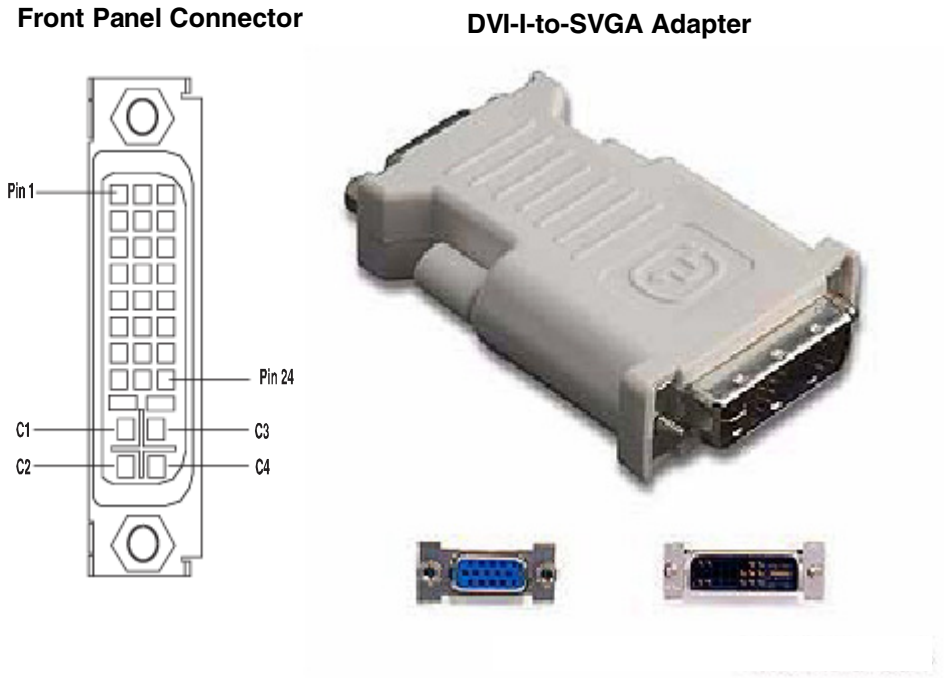


Table A-6 DVI-I Connector Pinout

Pin#	Signal Assignment	Pin#	Signal Assignment	Pin#	Signal Assignment
1	Data 2-	9	Data 1-	17	Data 0-
2	Data 2+	10	Data 1+	18	Data 0+
3	Data 2/4 Shield/GND	11	Data 1/3 Shield/GND	19	Data 0/5 Shield/GND
4	N/C	12	N/C	20	N/C
5	N/C	13	N/C	21	N/C
6	DDC Clock	14	+5VDC Power (750 mA)	22	Clock Shield/GND
7	DDC Data	15	GND (Return for +5, HSync and VSync)	23	Clock+
8	Analog VSync	16	Hot Plug Detect	24	Clock-
C1	Analog Red	C2	Analog Green	C3	Analog Blue
C4	Analog HSync	C5	Analog GND (RGB return)		

A.6 Keyboard and Mouse Connectors and Pinout (J6)

The keyboard and mouse connectors are standard 6-pin female mini-DIN PS/2 connectors as shown in the Figure and Table below.

Figure A-6 Keyboard/Mouse Connector

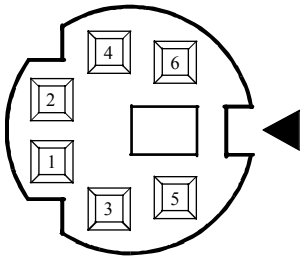


Table A-7 Keyboard/Mouse Connector*

Pin	Direction	Function
1	In/Out	Mouse Data
2	In/Out	Keyboard Data
3		Ground
4		+5V
5	Out	Mouse Clock
6	Out	Keyboard Clock
Shield		Chassis Ground

*An adapter cable is included with the VMIVME-7851/VME-7851RC to separate the keyboard and mouse connector.

Table A-8 Keyboard/Mouse Y Splitter Cable

Keyboard			Mouse		
Pin	Direction	Function	Pin	Direction	Function
1	In/Out	Keyboard Data	1	In/Out	Mouse Data
2		Unused	2		Keyboard Data
3		Ground	3		Ground
4		+5V	4		+5V
5	Out	Keyboard Clock	5	Out	Mouse Clock
6		Unused	6		Keyboard Clock
Shield		Chassis Ground	Shield		Chassis Ground

A.7 PMC Connector Pinouts

A.7.1 PMC #1 (J1) Main Board Connector and Pinout

The PMC carries the same signals as the PCI standard; however, the PMC standard uses a completely different form factor. Tables A-9 through A-11 are the pinouts for the PMC #1 connectors (J1, J2 and J3).

Figure A-7 PMC #1 (J1) Connector

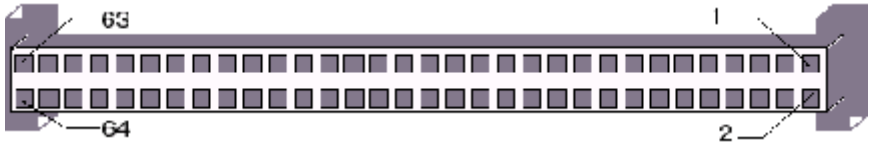


Table A-9 PMC #1 (J1) Connector Pinout

PMC Connector (J1)				PMC Connector (J1)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	+12V	2	+5V	33	GND	34	NC
3	GND	4	NC	35	TRDY	36	+3.3V
5	+5V	6	GND	37	GND	38	STOP#
7	GND	8	NC	39	PERR#	40	GND
9	NC	10	NC	41	+3.3V	42	SERR#
11	BMODE2#	12	+3.3V	43	C/BE1#	44	GND
13	RST#	14	BMODE3#	45	AD[14]	46	AD[13]
15	+3.3V	16	BMODE4#	47	GND	48	AD[10]
17	NC	18	GND	49	AD[8]	50	+3.3V
19	AD[30]	20	AD[29]	51	AD[7]	52	NC
21	GND	22	AD[26]	53	+3.3V	54	NC
23	AD[24]	24	+3.3V	55	NC	56	GND
25	IDSEL AD[31]	26	AD[23]	57	NC	58	NC
27	+3.3V	28	AD[20]	59	GND	60	NC
29	AD[18]	30	GND	61	ACK64#	62	+3.3V
31	AD[16]	32	C/BE2#	63	GND	64	NC

A.7.2 PMC #1 (J2) Main Board Connector and Pinout

Figure A-8 PMC #1 (J2) Connector

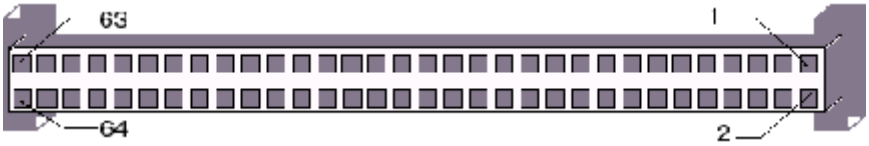


Table A-10 PMC #1 (J2) Connector Pinout

PMC Connector (J2)				PMC Connector (J2)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	GND	2	-12	33	FRAME#	34	GND
3	GND	4	PIRQC#	35	GND	36	IRDY#
5	PIRQD#	6	PIRQA#	37	DEVSEL#	38	+5V
7	BMODE1#	8	+5V	39	GND	40	LOCK#
9	PIRQB#	10	NC	41	SDONE#	42	4.7k pull-up
11	GND	12	NC	43	PAR	44	GND
13	CLK	14	GND	45	+5V	46	AD[15]
15	GND	16	GNT2#	47	AD[12]	48	AD[11]
17	REQ2#	18	+5V	49	AD[9]	50	+5V
19	+5V	20	AD[31]	51	GND	52	C/BE0#
21	AD[28]	22	AD[27]	53	AD[6]	54	AD[5]
23	AD[25]	24	GND	55	AD[4]	56	GND
25	GND	26	C/BE3#	57	+5V	58	AD[3]
27	AD[22]	28	AD[21]	59	AD[2]	60	AD[1]
29	AD[19]	30	+5V	61	AD[0]	62	+5V
31	+5V	32	AD[17]	63	GND	64	2.2k pull-up

A.7.3 PMC #1 (J3) Main Board Connector and Pinout

Figure A-9 PMC #1 (J3) Connector

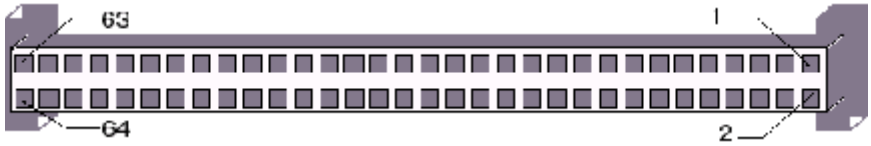


Table A-11 PMC #1 (J3) Connector Pinout

PMC Connector (J3)						PMC Connector (J3)					
Left Side			Right Side			Left Side			Right Side		
Pin	Name	Connected To	Pin	Name	Connected To	Pin	Name	Connected To	Pin	Name	Connected To
1	CONN[1]	P2 pin D1	2	CONN[2]	P2 pin Z1	33	CONN[33]	P2 pin D22	34	CONN[34]	P2 pin D23
3	CONN[3]	P2 pin D2	4	CONN[4]	P2 pin D3	35	CONN[35]	P2 pin Z23	36	CONN[36]	P2 pin D24
5	CONN[5]	P2 pin Z3	6	CONN[6]	P2 pin D4	37	CONN[37]	P2 pin D25	38	CONN[38]	P2 pin Z25
7	CONN[7]	P2 pin D5	8	CONN[8]	P2 pin Z5	39	CONN[39]	P2 pin D26	40	CONN[40]	P2 pin D27
9	CONN[9]	P2 pin D6	10	CONN[10]	P2 pin D7	41	CONN[41]	P2 pin Z27	42	CONN[42]	P2 pin D28
11	CONN[11]	P2 pin Z7	12	CONN[12]	P2 pin D8	43	CONN[43]	P2 pin D29	44	CONN[44]	P2 pin Z29
13	CONN[13]	P2 pin D9	14	CONN[14]	P2 pin Z9	45	CONN[45]	P2 pin D30	46	CONN[46]	P2 pin Z31
15	CONN[15]	P2 pin D10	16	CONN[16]	P2 pin D11	47	CONN[47]	NC	48	CONN[48]	NC
17	CONN[17]	P2 pin Z11	18	CONN[18]	P2 pin D12	49	CONN[49]	NC	50	CONN[50]	NC
19	CONN[19]	P2 pin D13	20	CONN[20]	P2 pin Z13	51	CONN[51]	NC	52	CONN[52]	NC
21	CONN[21]	P2 pin D14	22	CONN[22]	P2 pin D15	53	CONN[53]	NC	54	CONN[54]	NC
23	CONN[23]	P2 pin Z15	24	CONN[24]	P2 pin D16	55	CONN[55]	NC	56	CONN[56]	NC
25	CONN[25]	P2 pin D17	26	CONN[26]	P2 pin Z17	57	CONN[57]	NC	58	CONN[58]	NC
27	CONN[27]	P2 pin D18	28	CONN[28]	P2 pin D19	59	CONN[59]	NC	60	CONN[60]	NC
29	CONN[29]	P2 pin Z19	30	CONN[30]	P2 pin D20	61	CONN[61]	NC	62	CONN[62]	NC
31	CONN[31]	P2 pin D21	32	CONN[32]	P2 pin Z21	63	CONN[63]	NC	64	CONN[64]	NC

A.7.4 PMC #2 (J1) Expansion Board Connector and Pinout

The PMC carries the same signals as the PCI standard; however, the PMC standard uses a different form factor. Tables A-12 through A14 are the pinouts for the PMC #2 connectors (J1, J2 and J7).

Figure A-10 PMC #2 (J1) Connector

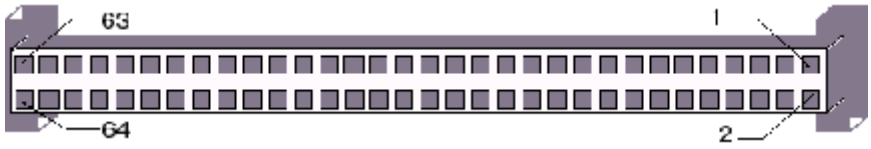


Table A-12 PMC #2 (J1) Connector Pinout

PMC Connector (J1)				PMC Connector (J1)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	GND	2	-12	33	FRAME#	34	GND
3	GND	4	PIRQG#	35	GND	36	IRDY#
5	PIRQH#	6	PIRQD#	37	DEVSEL#	38	+5V
7	NC	8	+5V	39	GND	40	LOCK#
9	PIRQF#	10	NC	41	2.2k pull-up	42	4.7k pull-up
11	GND	12	NC	43	PAR	44	GND
13	CLK	14	GND	45	+5V	46	AD[15]
15	GND	16	GNT4#	47	AD[12]	48	AD[11]
17	REQ4#	18	+5V	49	AD[9]	50	+5V
19	+5V	20	AD[31]	51	GND	52	C/BE0#
21	AD[28]	22	AD[27]	53	AD[6]	54	AD[5]
23	AD[25]	24	GND	55	AD[4]	56	GND
25	GND	26	C/BE3#	57	+5V	58	AD[3]
27	AD[22]	28	AD[21]	59	AD[2]	60	AD[1]
29	AD[19]	30	+5V	61	AD[0]	62	+5V
31	+5V	32	AD[17]	63	GND	64	2.2k pull-up

A.7.5 PMC #2 (J2) Extension Board Connector and Pinout

Figure A-11 PMC #2 (J2) Connector

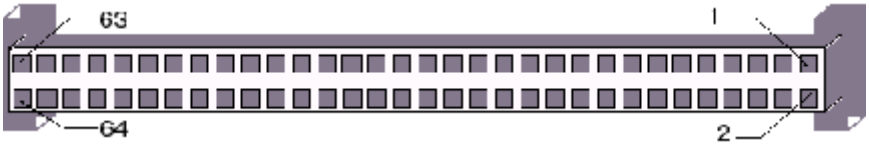


Table A-13 PMC #2 (J2) Connector Pinout

PMC Connector (J2)				PMC Connector (J2)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	+12V	2	+5V	33	GND	34	NC
3	GND	4	NC	35	TRDY	36	+3.3V
5	+5V	6	GND	37	GND	38	STOP#
7	GND	8	NC	39	PERR#	40	GND
9	NC	10	NC	41	+3.3V	42	SERR#
11	10k pull-up	12	+3.3V	43	C/BE1#	44	GND
13	RST#	14	220 Ohm pull-down	45	AD[14]	46	AD[13]
15	+3.3V	16	220 Ohm pull-down	47	GND	48	AD[10]
17	NC	18	GND	49	AD[8]	50	+3.3V
19	AD[30]	20	AD[29]	51	AD[7]	52	NC
21	GND	22	AD[26]	53	+3.3V	54	NC
23	AD[24]	24	+3.3V	55	NC	56	GND
25	IDSEL AD[18]	26	AD[23]	57	NC	58	NC
27	+3.3V	28	AD[20]	59	GND	60	NC
29	AD[18]	30	GND	61	2.2k pull-up	62	+3.3V
31	AD[16]	32	C/BE2#	63	GND	64	NC

A.7.6 PMC #2 (J7) Extension Board Connector and Pinout

Figure A-12 PMC #2 (J7) Connector

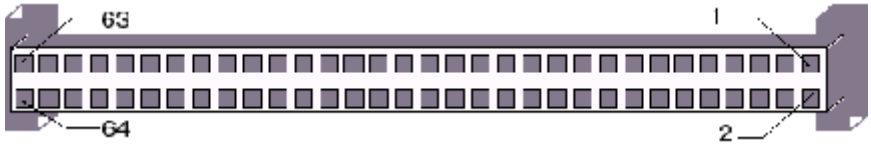


Table A-14 PMC #2 (J7) Connector Pinout

PMC Connector (J7)						PMC Connector (J7)					
Left Side			Right Side			Left Side			Right Side		
Pin	Name	Connected To	Pin	Name	Connected To	Pin	Name	Connected To	Pin	Name	Connected To
1	CONN[1]	P2 pin D1	2	CONN[2]	P2 pin Z1	33	CONN[33]	P2 pin D22	34	CONN[34]	P2 pin D23
3	CONN[3]	P2 pin D2	4	CONN[4]	P2 pin D3	35	CONN[35]	P2 pin Z23	36	CONN[36]	P2 pin D24
5	CONN[5]	P2 pin Z3	6	CONN[6]	P2 pin D4	37	CONN[37]	P2 pin D25	38	CONN[38]	P2 pin Z25
7	CONN[7]	P2 pin D5	8	CONN[8]	P2 pin Z5	39	CONN[39]	P2 pin D26	40	CONN[40]	P2 pin D27
9	CONN[9]	P2 pin D6	10	CONN[10]	P2 pin D7	41	CONN[41]	P2 pin Z27	42	CONN[42]	P2 pin D28
11	CONN[11]	P2 pin Z7	12	CONN[12]	P2 pin D8	43	CONN[43]	P2 pin D29	44	CONN[44]	P2 pin Z29
13	CONN[13]	P2 pin D9	14	CONN[14]	P2 pin Z9	45	CONN[45]	P2 pin D30	46	CONN[46]	P2 pin Z31
15	CONN[15]	P2 pin D10	16	CONN[16]	P2 pin D11	47	CONN[47]	P2 pin D31	48	CONN[48]	P2 pin D32
17	CONN[17]	P2 pin Z11	18	CONN[18]	P2 pin D12	49	CONN[49]	E8 pin 1*	50	CONN[50]	P2 pin A24
19	CONN[19]	P2 pin D13	20	CONN[20]	P2 pin Z13	51	CONN[51]	P2 pin C25	52	CONN[52]	P2 pin A25
21	CONN[21]	P2 pin D14	22	CONN[22]	P2 pin D15	53	CONN[53]	P2 pin C1	54	CONN[54]	P2 pin A13
23	CONN[23]	P2 pin Z15	24	CONN[24]	P2 pin D16	55	CONN[55]	E8 pin 2*	56	CONN[56]	P2 pin C13
25	CONN[25]	P2 pin D17	26	CONN[26]	P2 pin Z17	57	CONN[57]	E8 pin 4*	58	CONN[58]	P2 pin C29
27	CONN[27]	P2 pin D18	28	CONN[28]	P2 pin D19	59	CONN[59]	E8 pin 3*	60	CONN[60]	P2 pin C30
29	CONN[29]	P2 pin Z19	30	CONN[30]	P2 pin D20	61	CONN[61]	P2 pin C31	62	CONN[62]	P2 pin A30
31	CONN[31]	P2 pin D21	32	CONN[32]	P2 pin Z21	63	CONN[63]	P2 pin C32	64	CONN[64]	P2 pin A31

*These signals do not go to P2, but rather a 2x2 header (E8).

A.7.7 PMC #3 (J3) Main Board Connector and Pinout

The PMC carries the same signals as the PCI standard; however, the PMC standard uses a completely different form factor. Tables A-15 through A-16 are the pinouts for the PMC #3 connectors.

Figure A-13 PMC #3 (J3) Connector

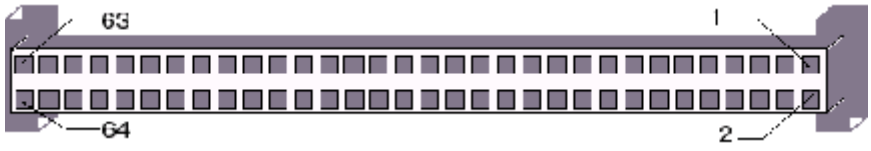


Table A-15 PMC #3 (J3) Connector Pinout

PMC Connector (J3)				PMC Connector (J3)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	GND	2	-12	33	FRAME#	34	GND
3	GND	4	PIRQH#	35	GND	36	IRDY#
5	PIRQF#	6	PIRQD#	37	DEVSEL#	38	+5V
7	NC	8	+5V	39	GND	40	LOCK#
9	PIRQG	10	NC	41	2.2k pull-up	42	4.7k pull-up
11	GND	12	NC	43	PAR	44	GND
13	CLK	14	GND	45	+5V	46	AD[15]
15	GND	16	GNT5#	47	AD[12]	48	AD[11]
17	REQ5#	18	+5V	49	AD[9]	50	+5V
19	+5V	20	AD[31]	51	GND	52	C/BE0#
21	AD[28]	22	AD[27]	53	AD[6]	54	AD[5]
23	AD[25]	24	GND	55	AD[4]	56	GND
25	GND	26	C/BE3#	57	+5V	58	AD[3]
27	AD[22]	28	AD[21]	59	AD[2]	60	AD[1]
29	AD[19]	30	+5V	61	AD[0]	62	+5V
31	+5V	32	AD[17]	63	GND	64	2.2k pull-up

A.7.8 PMC #3 (J4) Extension Board Connector and Pinout

Figure A-14 PMC #3 (J4) Connector

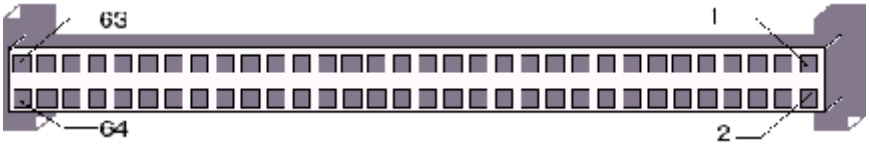


Table A-16 PMC #3 (J4) Connector Pinout

PMC Connector (J4)				PMC Connector (J4)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	+12V	2	+5V	33	GND	34	NC
3	GND	4	NC	35	TRDY	36	+3.3V
5	+5V	6	GND	37	GND	38	STOP#
7	GND	8	NC	39	PERR#	40	GND
9	NC	10	NC	41	+3.3V	42	SERR#
11	10k pull-up	12	+3.3V	43	C/BE1#	44	GND
13	RST#	14	220 Ohm pull-down	45	AD[14]	46	AD[13]
15	+3.3V	16	220 Ohm pull-down	47	GND	48	AD[10]
17	NC	18	GND	49	AD[8]	50	+3.3V
19	AD[30]	20	AD[29]	51	AD[7]	52	NC
21	GND	22	AD[26]	53	+3.3V	54	NC
23	AD[24]	24	+3.3V	55	NC	56	GND
25	IDSEL AD[21]	26	AD[23]	57	NC	58	NC
27	+3.3V	28	AD[20]	59	GND	60	NC
29	AD[18]	30	GND	61	2.2k pull-up	62	+3.3V
31	AD[16]	32	C/BE2#	63	GND	64	NC

A.8 Optional SCSI Pinout (J5)

The optional Dual Ultra160 SCSI devices use a high density connector AMP-787962-1. The pinout for this connector is shown below.

Table A-17 Optional (J5) SCSI Pinout

Channel A External				Channel B External			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1A	A_SD(12)+	2A	A_SD(13)+	1B	B_SD(12)+	2B	B_SD(13)+
3A	A_SD(14)+	4A	A_SD(15)+	3B	B_SD(14)+	4B	B_SD(15)+
5A	A_SDP1+	6A	A_SD(0)+	5B	B_SDP1+	6B	B_SD(0)+
7A	A_SD(1)+	8A	A_SD(2)+	7B	B_SD(1)+	8B	B_SD(2)+
9A	A_SD(3)+	10A	A_SD(4)+	9B	B_SD(3)+	10B	B_SD(4)+
11A	A_SD(5)+	12A	A_SD(6)+	11B	B_SD(5)+	12B	B_SD(6)+
13A	A_SD(7)+	14A	A_SDP0+	13B	B_SD(7)+	14B	B_SDP0+
15A	GND	16A	A_DIFFSEN	15B	GND	16B	B_DIFFSEN
17A	A_TERMPWR_EX	18A	A_TERMPWR_EX	17B	B_TERMPWR_EX	18B	B_TERMPWR_EX
19A	N/C	20A	GND	19B	N/C	20B	GND
21A	A_SATN+	22A	GND	21B	B_SATN+	22B	GND
23A	A_SBSY+	24A	A_SACK+	23B	B_SBSY+	24B	B_SACK+
25A	A_SRST+	26A	A_SMSG+	25B	B_SRST+	26B	B_SMSG+
27A	A_SSEL+	28A	A_SC_D+	27B	B_SSEL+	28B	B_SC_D+
29A	A_SREQ+	30A	A_SI_O+	29B	B_SREQ+	30B	B_SI_O+
31A	A_SD(8)+	32A	A_SD(9)+	31B	B_SD(8)+	32B	B_SD(9)+
33A	A_SD(10)+	34A	A_SD(11)+	33B	B_SD(10)+	34B	B_SD(11)+
35A	A_SD(12)-	36A	A_SD(13)-	35B	B_SD(12)-	36B	B_SD(13)-
37A	A_SD(14)-	38A	A_SD(15)-	37B	B_SD(14)-	38B	B_SD(15)-
39A	A_SDP1-	40A	A_SD(0)-	39B	B_SDP1-	40B	B_SD(0)-
41A	A_SD(1)-	42A	A_SD(2)-	41B	B_SD(1)-	42B	B_SD(2)-
43A	A_SD(3)-	44A	A_SD(4)-	43B	B_SD(3)-	44B	B_SD(4)-
45A	A_SD(5)-	46A	A_SD(6)-	45B	B_SD(5)-	46B	B_SD(6)-
47A	A_SD(7)-	48A	A_SDP0-	47B	B_SD(7)-	48B	B_SDP0-
49A	GND	50A	NC	49B	GND	50B	NC
51A	A_TERMPWR_EX	52A	A_TERMPWR_EX	51B	B_TERMPWR_EX	52B	B_TERMPWR_EX
53A	N/C	54A	GND	53B	N/C	54B	GND
55A	A_SATN-	56A	GND	55B	B_SATN-	56B	GND
57A	A_SBSY-	58A	A_SACK-	57B	B_SBSY-	58B	B_SACK-
59A	A_SRST-	60A	A_SMSG-	59B	B_SRST-	60B	B_SMSG-
61A	A_SSEL-	62A	A_SC_D-	61B	B_SSEL-	62B	B_SC_D-
63A	A_SREQ-	64A	A_SI_0-	63B	B_SREQ-	64B	B_SI_0-
65A	A_SD(8)-	66A	A_SD(9)-	65B	B_SD(8)-	66B	B_SD(9)-
67A	A_SD(10)-	68A	A_SD(11)-	67B	B_SD(10)-	68B	B_SD(11)-

B • Appendix B: System Driver Software

The VMIVME-7851/VME-7851RC provide high-performance video and Local Area Network (LAN) access by means of the onboard Intel 82852GM chipset and either an Intel 82540EM Gigabit Ethernet chip for the VMIVME-7851 or an Intel 82541PI Gigabit Ethernet chip for the VME-7851RC. The two LAN adapters can be configured to allow the VMIVME-7851/VME-7851RC access to two separate, physical networks. One LAN adapter is capable of running 10Base-T and 100Base-TX and the other is the Gbit Ethernet adapter (1000Mb/s).

To optimize performance of each of these PCI-based subsystems, install the driver software located on the distribution CD-ROM provided with the unit. Detailed instructions for installation of the drivers during the installation of Microsoft Windows XP Professional and Windows 2000 operating systems are provided in the following sections.

B.1 Windows 2000

B.1.1 Ultra160 SCSI Driver Disk Preparation (Optional)

The SCSI driver for Windows 2000 Professional is provided on the 385-000114-000 CD-ROM. Before attempting the installation of the operating system onto a SCSI device, the appropriate driver files must be copied to a blank, user-supplied floppy disk. This driver disk will be used at the beginning of the Windows 2000 installation.

To create a Windows 2000 driver disk, browse to the \Win2K\SCSI\ directory on the 385-000114-000 CD-ROM. Copy all files and directories to the root directory of a blank floppy disk. Label the disk 'Symbios Ultra3 PCI SCSI Driver'.

B.1.2 INF Update

1. Follow normal Windows 2000 installation procedures.
2. Insert **CD-ROM 385-000114-000**.
3. Double click on **My Computer.**
4. Double click on the **CD-ROM** drive containing the CD-ROM inserted earlier.
5. Double click on the **Win2K folder**.
6. Double click on **INF Update Utility**.
7. At the InstallShield Wizard window, click **Next**.
   Click **Yes** to agree to the license agreement.
   Click **Next**.
   Select **Yes, I want to restart my computer now** after files have been installed,
   Click **Finish**. Allow Windows to restart.

B.1.3 Video Driver

1. Insert **CD-ROM 385-000114-000**.
2. Double click on **My Computer.**
3. Double click on the **CD-ROM drive** containing the CD-ROM inserted earlier.
4. Double click on the **Win2K folder**.
5. Double click on **Video**.
6. At the InstallShield Wizard, click **Next**.
   Click **Next** after files have been extracted
   Click **Yes** to agree to the license agreement.
   Select **Yes, I want to restart my computer now** after files have been installed,
   Click **Finish**. Allow Windows to restart.

B.1.4 Ethernet Drivers

1. Insert **CD-ROM 385-000114-000**.
2. Right click on **My Computer** and select **Manage**.
3. Select **Device Manager** in the left pane of the Computer Management window.
4. Double click on the first **Ethernet Controller** under *Other Devices* in the right pane.
5. Click the **Reinstall Driver** button.
6. Click **Next**.
7. Select **Search for a suitable driver for my device** and click **Next**.
8. Deselect **Floppy disk drives** and select **Specify a location**.
9. Click **Next**.
10. Click the **Browse** button and browse to the root of the CD-ROM inserted earlier.
11. Browse into the **Win2K folder** and then into the **i82540EM Gigabit LAN folder.**
12. Click **Open**.
13. Click **OK**.
14. Click **Next**.
15. Click **Finish** after files have been installed.
16. Click **Close**.
17. Double click on the remaining **Ethernet Controller** in the right pane.
18. Click the **Reinstall Driver** button.
19. Click **Next**.
20. Select **Search for a suitable driver for my device** and click **Next**.
21. Deselect **Floppy disk drives** and select **Specify a location**.
22. Click **Next**.
23. Click the **Browse** button and browse to the root of the CD-ROM inserted earlier.
24. Browse into the **Win2K folder** and then into the **i82852 Internal LAN folder**.
25. Click **Open**.
26. Click **OK**.
27. Click **Next**.
28. Click **Finish** after files have been installed.
29. Click **Close**.
30. Click **X** to close the *Computer Management* window.

B.1.5 SCSI Driver

NOTE

If the SCSI driver was loaded during OS installation, this section may be skipped.

1. Insert **CD-ROM 385-000114-000**.
2. Right click on **My Computer** and select **Manage**.
3. Select **Device Manager** in the left pane of the Computer Management window
4. Double click on the first **SCSI Controller** under *Other Devices* in the right pane.
5. Click the **Reinstall Driver** button.
6. Click **Next**.
7. Select **Search for a suitable driver for my device** and click **Next**.
8. Deselect **Floppy disk drives** and select **Specify a location**.
9. Click **Next**.
10. Click the **Browse** button and browse to the root of the CD-ROM inserted earlier.
11. Browse into the **Win2K folder**, into the **SCSI folder,** into the **WinNT**, and into the **MiniPort folder**.
12. Click **Open**.
13. Click **OK**.
14. Click **Next**.
15. Click **Yes** at the *Digital Signature Not Found* window.
16. Click **Finish** after files have been installed.
17. Click **Close**.
18. Repeat steps 4 through 17 for the remaining SCSI Controller.
19. Click **X** to close the *Computer Management* window.

B.2 Windows XP

B.2.1 INF Update

1. Follow normal Windows XP installation procedures.
2. Insert **CD-ROM 385-000114-000**.
3. Click on **Start**, *My Computer*.
4. Double click on the **CD-ROM drive** containing the CD-ROM inserted earlier.
5. Double click on the **WinXP folder.**
6. Double click on **INF Update Utility**.
7. Click **Next** at the *InstallShield Wizard* window.
   Click **Yes** to agree to the license agreement.
   Click **Next**.
   Select **Yes, I want to restart my computer now** after files have been installed.
   Click **Finish**. Allow Windows to restart.

B.2.2 Video Driver

1. Insert **CD-ROM 385-000114-000**.
2. Click on **Start**, *My Computer.*
3. Double click on the **CD-ROM drive** containing the CD-ROM inserted earlier.
4. Double click on the **WinXP folder**.
5. Double click on **Video**.
6. Click **Next** at the *InstallShield Wizard*.
   Click **Next** after files have been extracted.
   Click **Yes** to agree to the license agreement.
   Select **Yes, I want to restart my computer now** after hardware has been detected and files installed.
   Click **Finish**. Allow Windows to restart.

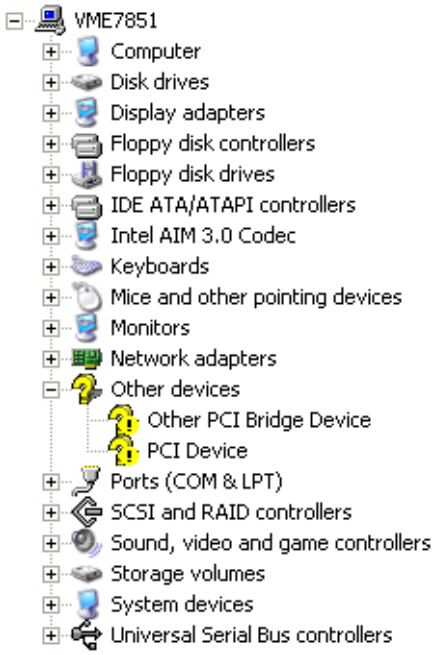
B.2.3 Ethernet Drivers

1. Insert **CD-ROM 385-000114-000**.
2. Click on **Start**. Right click on *My Computer* and select **Manage**.
3. Select **Device Manager** in the left pane of the *Computer Management window.*
4. Double click on the first **Ethernet Controller** under *Other Devices* in the right pane.
5. Click the **Reinstall Driver** button.
6. Select **No, not this time** and click **Next**.
7. Select **Install the software automatically (Recommended)** and click **Next**.
8. Click **Finish** after the files have been installed.
9. Click **Close**.
10. Click **X** to close the *Computer Management* window.

B.3 Status of PCI Devices Listed in Windows Device Manager

After installing all of the drivers provided on the Windows Drivers CD-ROM, Device Manager will still indicate that several PCI devices do not have drivers loaded. In the sample screen shot shown in Figure B-1, the two devices listed under “Other devices” are the Tundra Universe IIB PCI-to-VME bridge and the GE proprietary FPGA. Although these devices are listed as non-functioning by Windows, the hardware is functioning as designed.

Figure B-1 Device Manager



C • Appendix C: Argon BIOS

The VMIVME-7851/VME-7851RC include an Argon BIOS option which allows the SBCs to be booted from a network. This appendix describes the procedures to enable this option and the Argon BIOS Setup screens.

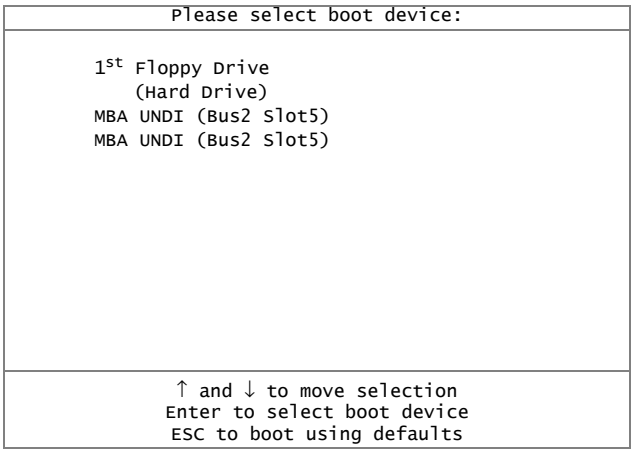
C.1 Boot Menus

There are two methods of enabling the Argon BIOS option. The first method is the *First Boot* menu. The second is the *Boot* menu from the BIOS Setup Utility.

C.1.1 First Boot Menu

Press F11 at the very beginning of the boot cycle, which will access the *First Boot* menu. Selecting *Managed PC Boot Agent (MBA)* to boot from the LAN in this screen applies to the current boot only. At the next reboot the VMIVME-7851/VME-7851RC will revert back to the setting in the Boot menu.

Table C-1 Argon BIOS First Boot Menu



Using the arrow keys, highlight *Managed PC Boot Agent (MBA)*, and press the **ENTER** key to continue with the system boot.

C.1.2 Boot Menu

The second method of enabling the Argon BIOS option is to press the DEL key during system boot. This will access the *BIOS Setup Utility*. Advance to the *Boot* menu, and to the *Boot Device Priority* sub-menu. Use the arrow keys to highlight the *Managed PC Boot Agent (MBA)* option. Repeat entering <+> until the desired MBA is at the top of the list.

Advance to the *Exit* menu, select *Exit Saving Changes* and press **ENTER**. When the system prompts for confirmation, press *Yes*. The computer will then restart the system bootup.

Table C-2 Argon BIOS Boot Menu

BIOS SETUP UTILITY		
	Boot	
Boot Device Priority		Specifies the boot sequence from the available devices.
1st Boot Device 2nd Boot Device 3rd Boot Device	[MBA UNDI (Bus2 Slot5)] [1st Floppy Drive] [Hard Drive]	←→ Select Screen ↑↓ Select Item +- Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit

C.2 BIOS Features Setup Menu

After the Managed PC Boot Agent has been enabled, there are several boot options available to the user. These options are RPL (default), TCP/IP, Netware and PXE. The proceeding screen shots show the defaults for each boot method.

C.2.1 RPL Menu

Table C-3 RPL Default Settings

```
Argon Managed PC Boot Agent (MBA) v4.00 (BIOS Integrated)
(c) Copyright 2002 Argon Technology Corporation
All rights reserved
```

```
                              Configuration

    Boot Method:              RPL

    Config Message:           Enabled
    Message Timeout:          3 Seconds
    Boot failure Prompt:      Wait for timeout
    Boot Failure:             Next boot device
```

```
Use cursor keys to edit: Up/Down change field, Left/Right change value
ESC to quit, F9 restore previous settings, F10 to save
```

C.2.2 TCP/IP Menu

Table C-4 TCP/IP Default Settings

```
   Argon Managed PC Boot Agent (MBA) v4.00 (BIOS Integrated)
   (c) Copyright 2002 Argon Technology Corporation
   All rights reserved
```

```
                                Configuration

      Boot Method:              TCP/IP

      Protocol                  DHCP
      Config Message:           Enabled
      Message Timeout:          3 Seconds
      Boot failure Prompt:      Wait for timeout
      Boot Failure:             Next boot device
```

```
Use cursor keys to edit: Up/Down change field, Left/Right change value
ESC to quit, F9 restore previous settings, F10 to save
```

C.2.3 Netware Menu

Table C-5 Netware Default Settings

```
   Argon Managed PC Boot Agent (MBA) v4.00 (BIOS Integrated)
   (c) Copyright 2002 Argon Technology Corporation
   All rights reserved
```

```
                                Configuration

      Boot Method:              Netware

      Protocol                  802.3
      Config Message:           Enabled
      Message Timeout:          3 Seconds
      Boot failure Prompt:      Wait for timeout
      Boot Failure:             Next boot device
```

```
Use cursor keys to edit: Up/Down change field, Left/Right change value
ESC to quit, F9 restore previous settings, F10 to save
```

C.2.4 PXE Menu

Table C-6 PXE Default Settings

```
Argon Managed PC Boot Agent (MBA) v4.00 (BIOS Integrated)
(c) Copyright 2002 Argon Technology Corporation
All rights reserved
```

```
                                Configuration

      Boot Method:              PXE

      Config Message:           Enabled
      Message Timeout:          3 Seconds
      Boot Failure Prompt:      Wait for timeout
      Boot Failure:             Next boot device
```

```
Use cursor keys to edit: Up/Down change field, Left/Right change value
ESC to quit, F9 restore previous settings, F10 to save
```

D • Appendix D: SCSI BIOS

The VMIVME-7851/VME-7851RC are optionally available with a dual channel LSI53C1010 SCSI adapter. When this option is loaded, the SDMS SCSI BIOS and Configuration Utility will be accessible for user configuration.

This section presents general information about the SDMS SCSI BIOS and Configuration Utility Version 4.19.00.

A SCSI BIOS is the bootable ROM code that manages SCSI hardware resources. It is specific to a family of LSI Logic SCSI controllers or processors. An SDMS SCSI BIOS integrates with a standard system BIOS, extending the standard disk service routine provided through INT13h.

During the boot time initialization, the SCSI BIOS determines if there are other hard disks, such as an IDE drive, already installed by the system BIOS.

If there are, the SCSI BIOS maps any SCSI drives it finds behind the drive(s) already installed. Otherwise, the SCSI BIOS installs drives starting with the system boot drive. In this case, the system boots from a drive controlled by the SCSI BIOS. For 4.05 versions and higher, LSI Logic supports the BIOS Boot Specification (BBS). The section below, ***D.2 Boot Initialization with BIOS Boot Specification (BBS),*** discusses selecting boot and drive order.

NOTE

In order to boot from SCSI devices, some operating systems require that the SCSI driver be set to "boot" within the Control Panel.

D.1 Features

The SDMS SCSI BIOS features include:

- Configuration for up to 256 adapters - any four can be chosen for INT13 (bootrom) support.
- All LSI53C8xx devices including LSI53C895A.
- LSI53C1510 device.
- LSI53C1010 device.
- SPI-3 Parallel Protocol Request (PPR).
- Basic Domain Validation.

D.2 Boot Initialization with BIOS Boot Specification (BBS)

The SDMS SCSI BIOS provides support for the BBS, which allows you to choose which device to boot from by selecting the priority.

The system BIOS present on the VMIVME-7851/VME-7851RC is compatible with the BBS. Use the system BIOS setup menu to select the boot and drive order. In the system BIOS setup, the Boot Connection Devices menu appears with a list of available boot options. Use this menu to select the device and rearrange the order, then exit to continue the boot process.

D.2.1 CD-ROM Boot Initialization

The SDMS SCSI BIOS supports boot initialization from a CD-ROM drive. The five types of emulation are:

- No emulation disk
- Floppy 1.2MB emulation disk
- Floppy 1.44MB emulation disk
- Floppy 2.88MB emulation disk
- Hard disk emulation

The type of emulation assigns the drive letter for the CD-ROM. For example, if a 1.44MB floppy emulation CD-ROM was loaded, then the CD-ROM drive would become the designated A drive, and the existing floppy would become drive B.

D.2.2 Starting the SCSI BIOS Configuration Utility

If you have SCSI BIOS version 4.XX, and it includes the SDMS SCSI BIOS Configuration Utility, you can change the default configuration of your SCSI host adapters. You may decide to alter these default values if there is a conflict between device settings or if you need to optimize system performance.

You can see the version number of the SCSI BIOS in a banner displayed on your computer monitor during boot. If the utility is available, this message also appears on your monitor:

Press Ctrl-C to start Symbios Configuration Utility...

This message remains on your screen for about five seconds, giving you time to start the utility. If you decide to press "Ctrl-C", the message changes to:

Please wait, invoking Symbios Configuration Utility...

After a brief pause, your computer monitor displays the Main menu of the Symbios SDMS PCI SCSI BIOS Configuration Utility.

To make changes with this menu driven utility, one or more SDMS SCSI host adapters must have NVRAM to store the changes.

These messages may appear during the boot process:

"Adapter removed from boot order, parameters will be updated accordingly" appears when an adapter is removed from the system or relocated behind a PCI bridge.

"Configuration data invalid, saving default configuration!" appears if none of the information in the NVRAM is valid.

"Found SCSI Controller not in following Boot Order List, to Add: Press Ctrl-C to start Symbios Configuration Utility..." or "Adapter configuration may have changed, reconfiguration is suggested!" could appear when fewer than four adapters are in the boot order and adapters exist in the system which are not in the boot order.

NOTE

The SCSI BIOS Configuration Utility is a powerful tool. If, while using it, you somehow disable all of your controllers, pressing Ctrl-A (or Ctrl-E on version 4.04 or later) after memory initialization during reboot allows you to re-enable and reconfigure. Also, if the system locks up due to NonVolatile Storage (NVS), press Ctrl-N to bypass the BIOS in order to reflash the card.

Not all devices detected by the SCSI BIOS Configuration Utility can be controlled by the BIOS. Devices such as tape drives and scanners require that a device driver specific to that peripheral be loaded. The SCSI BIOS Configuration Utility does allow parameters to be modified for these devices.

D.2.3 Using the Configuration Utility

Screen Format

All SCSI BIOS Configuration Utility screens are partitioned into fixed areas as shown below.

Table D-1 SCSI BIOS Configuration Utility Screen Partitions

Header Area							
MenuArea							
Adapter	PCI Bus	Dev/ Func	Port Number	IRQ	NVM	Boot Order	LSI Logic Control

F1 =Help	Arrow Keys =Select Item	-/+ =Change [Item]
Esc =Abort/ Exit		
F2 =Menu	Home/End =Select Item	Enter =Execute <Item>

Header Area

This area provides static information text, which is typically the product title and version.

Menu Area

This area provides the current Main Area's menu, if any. Press F2 to obtain a cursor for menu item selection.

Main Area

This is the main area for presenting data. This area has a cursor for item selection, horizontal scrolling and vertical scrolling. The horizontal and vertical scroll bars appear here.

Footer Area

This area provides general help information text.

User Input

Throughout these screens, selections that are not permissible are grayed out.

F1 = Help	Context sensitive help for the cursor-resident field.
F2 = Menu	Sets cursor context to the menu selection area. Select a menu item and press **Enter**.
Arrow Keys =	Up, down, left, right movement to position the cursor.
Home/End =	Select Item
+/- = Change [Item]	Items with values in [] brackets are modifiable. Use the '+' or '-' keys in the top row of the main keyboard or use the numeric keypad '+' and '-' keys to change a modifiable field. When pressed, they toggle a modifiable field to its next relative value. For example, '+' toggles the value up and '-' toggles the value down.
Esc = Abort/Exit	Escape aborts the current context operation and/or exits the current screen. User confirmation is solicited as required.
Enter = Execute <Item>	Items with values in <> brackets are executable. Press **Enter** to execute the field's associated function.

Main Menu

When you invoke the SDMS SCSI BIOS Configuration Utility, the Main menu appears. This menu displays a scrolling list of up to 256 LSI Logic PCI to SCSI host adapters in the system and information about each of them.

Use the arrow keys to select an adapter, then press **Enter** to view and modify the selected adapter's properties (and to gain access to the attached devices).

Only adapters with LSI Logic Control enabled can be accessed. Adapters with no NVM will show default settings and cannot be changed. After selecting an adapter and pressing Enter, the adapter's SCSI bus is scanned and the Adapter Properties menu appears. An example is shown after the descriptions about the Boot Adapter List and Global Properties menus.

On the Main menu, two selections are: Boot Adapter List and Global Properties. Press F2 to access these menus, use the arrow keys to select the desired menu, and press **Enter**.

“Boot Adapter List” allows selection and ordering of boot adapters.

“Global Properties” allows changes to global scope settings.

To execute an item, select it and press **Enter**. Here is an example of the Main menu:

Table D-2 Symbios SDMS (TM) PCI SCSI Configuration Utility Version PCI-4.19.00

<Boot Adapter List> <Global Properties>

Symbios Host Bus Adapters

Adapter	PCI Bus	Dev/ Func	Port Number	IRQ	NVM	Boot Order	Symbios Control
<53C1010-66	1	9>	D000	10	Yes	1	Enabled
<53C1010-66	1	8>	C000	11	Yes	0	Enabled

F1 =Help	Arrow Keys =Select Item	-/+ =Change [Item]
Esc =Abort/Exit F2 =Menu	Home/End =Select Item	Enter =Execute <Item>

D.2.4 Field Descriptions

Adapter

Indicates the specific family of LSI Logic Host Adapters.

PCI Bus

Indicates the PCI Bus number (range 0x00 - 0xFF, 0 - 255 decimal) assigned by the system BIOS to an adapter.

Dev/Func

Indicates the PCI Device/Function assigned by the system BIOS to an adapter.

An 8-bit value mapped as follows:

Bit # 7 6 5 4 3 2 1 0

> Bits 2-0: Function (range 0 - 7)

> Bits 7-3: Device (range 0x00 - 0x1F, 0 - 31 decimal).

Port Number

Indicates the I/O Port Number that communicates with an adapter. The system BIOS assigns this number.

IRQ

Indicates the Interrupt Request Line used by an adapter. The system BIOS also assigns this value.

NVM

Indicates whether an adapter has non-volatile memory (NVM) associated with it. An adapter's configuration is stored in its associated NVM. NVM can refer to NVRAM that is resident on a host adapter or to system NVM.

Boot Order

Indicates the relative boot order (0 to 3) of an adapter. The SDMS SCSI BIOS traverses up to four adapters in the specified order in search of bootable media. Access the "Boot Adapter List" Menu to modify this item.

LSI Logic Control

Indicates whether an adapter is eligible for LSI Logic software control, or is reserved for control by non-LSI Logic software.

D.2.5 Boot Adapter List

The Boot Adapter List menu specifies the order in which adapters will boot when more than one LSI Logic adapter is in a system. Up to four of the total adapters in a system can be selected as bootable. Adapters can be added or deleted using this menu.

To add an adapter to the boot list, press the Insert key while on the Boot Adapter List. This puts the cursor on the adapter select list. Use the arrow keys to select the desired adapter and press **Enter** to add it to the end of Boot Adapter List.

To remove an adapter from the boot list, press the Delete key while on the desired adapter in the Boot Adapter List. You can also change the boot order by using the '+' or '-' keys. For example, place the cursor on the adapter that you want to change, and use the '+' or '-' key to raise or lower the boot order.

The following is an example of the Boot Adapter List menu:

Table D-3 Symbios SDMS (TM) PCI SCSI Configuration Utility Version PCI-4.19.00

Boot Adapter List

Insert=Add an adapter		Delete=Remove an adapter			
Adapter	PCI Bus	Dev/ Func	Boot Order	Current Status	Next Boot
53C1010-66	1	68>	[0]	On	[On]
53C1010-66	1	69>	[1]	On	[On]

Hit Insert to select an adapter from this list:

<53C1010-66	1	9>
<53C1010-66	1	8>

F1 =Help	Arrow Keys =Select Item	-/+ =Change [Item]
Esc =Abort/Exit F2 =Menu	Home/End =Select Item	Enter =Execute <Item>

D.2.6 Field Descriptions

Adapter

Indicates the specific family of LSI Logic Host Bus Adapters.

PCI Bus

Indicates the PCI Bus number (range 0x00 - 0xFF, 0 - 255 decimal) assigned by the system BIOS to an adapter.

Dev/Func

Indicates the PCI Device/Function assigned by the system BIOS to an adapter.

Dev/Func	Indicates the PCI Device/Function assigned by the system BIOS to an adapter. An 8-bit value mapped as follows: Bit # 7 6 5 4 3 2 1 0 > Bits 2-0: Function (range 0 - 7) > Bits 7-3: Device (range 0x00 - 0x1F, 0 - 31 decimal).

Boot Order

Specifies the relative boot order (0 to 3) of an adapter.

- \- : decreases an adapter's relative boot order.
- \+ : increases an adapter's relative boot order.

Current Status

Indicates whether an adapter in the boot list was enabled during the most recent boot. Disabled adapters and their attached devices are ignored by the SDMS SCSI BIOS; they are still visible to the configuration utility.

Next Boot

Specifies whether to enable an adapter upon the next boot. The SDMS SCSI BIOS ignores disabled adapters and their attached devices although they are still visible to the configuration utility.

D.2.7 Global Properties

The Global Properties option on the Main menu provides additional properties that are not associated with a specific adapter or device. This menu allows you to view boot information, set display and video modes, pause if an alert message has been displayed, and set other options. Here is an example of the Global Properties menu:

Table D-4 Symbios SDMS (TM) PCI SCSI Configuration Utility Version PCI-4.19.00

Global Properties	
Pause When Boot Alert Displayed	[No]
Boot Information Display Mode	[Verbose]
Negotiate with devices	[Supported]
Video Mode	[Color]
Support Interrupt	[Hook interrupt, the Default]
<Restore Defaults>	

F1 =Help	Arrow Keys =Select Item	-/+ =Change [Item]
Esc =Abort/Exit F2 =Menu	Home/End =Select Item	Enter =Execute <Item>

D.2.8 Field Descriptions

Pause When Boot Alert Displayed

This option specifies whether to pause for user acknowledgment after displaying an alert message during boot. The Boot Alert setting can be either No or Yes. To continue after displaying a message, specify No. To wait for any key after displaying a message, specify Yes.

Boot Information Display Mode

This option specifies the information display mode of the BIOS during boot. It controls how much information about adapters and devices are displayed during boot. The Display Mode setting can be either Terse or Verbose. To display minimum information, specify Terse mode. To display detailed information, specify Verbose mode.

Negotiate With Devices

This option sets the default value for synchronous and wide negotiations with specified devices. Options are: All, None or Supported.

Video Mode

This option specifies the default video mode for the SCSI BIOS Configuration Utility. The Video Mode setting can be either Color or Monochrome. The monochrome setting enhances readability on a monochrome monitor.

Support Interrupt

This option allows the ability to prevent a hook on INT40, if required. The two settings are: Hook Interrupt (the default) and Bypass Interrupt Hook. Hook Interrupt is the normal operation that supports booting CD-ROMs in floppy emulation mode on most machines.

On certain platforms, the system BIOS uses the INT40h interrupt chain in a non-standard way. On these platforms, you should use the "Bypass Interrupt Hook" setting. This setting prevents a hook into the INT40h chain. If the "Bypass Interrupt Hook" setting is used on systems that do not require it, the CD-ROM may fail to boot and an error message may appear and indicate it is unable to read the boot device.

NOTE

Try toggling this value if your machine fails to boot a CD-ROM in floppy emulation mode.

Restore Defaults

Press **`Enter`** to obtain default settings.

D.2.9 Adapter Properties

The Adapter Properties menu allows you to view and modify adapter settings and SCSI devices connected to it. It also provides access to an adapter's device settings. To display this menu, select a device under the Adapter field on the Main menu and press Enter. Here is an example of the Adapter Properties menu:

Table D-5 Symbios SDMS (TM) PCI SCSI Configuration Utility Version PCI-4.19.00

Adapter Properties			
Adapter	PCI Bus	Dev/ Func	
53C1010-66	1	9	
	<Device Properties>		
	SCSI Parity		[Yes]
	Host SCSI ID		[7]
	SCSI Bus Scan Order		[Low to High (0..Max)]
	Removable Media Support		[None]
	CHS Mapping		[SCSI Plug and Play Mapping]
	Spinup Delay (Secs)		[2]
	Secondary Cluster Server		[No]
	Termination Control		[Auto]
	<Restore Defaults>		
F1 =Help	Arrow Keys =Select Item		-/+ =Change [Item]
Esc =Abort/Exit	Home/End =Select Item		Enter =Execute <Item>

D.3 Field Descriptions

If the field displays in grey or yellow text, it is available for changes. If it displays in white text, it is not available.

Device Properties

This option allows you to view and modify device properties. The Device Properties menu appears. Go to the next section for information about this menu.

SCSI Parity

This field indicates whether SCSI parity is enabled for an adapter. When disabled, it is also necessary to disable disconnects for all devices, as parity checking for the reselection phase is NOT disabled. If a non-parity generating device disconnects, its operation will never complete because the reselection fails due to parity error.

Host SCSI ID

This field indicates the SCSI identifier of an adapter [0-7] or [0-15]. It is recommended that this field be set to the highest priority SCSI identifier, which is 7.


NOTE

8-bit SCSI devices cannot see identifiers greater than 7.

SCSI Bus Scan Order

This field indicates the order in which to scan SCSI identifiers on an adapter. Changing this item will affect drive letter assignment(s) if more than one device is attached to an adapter.


NOTE

Changing this item may conflict with an operating system that automatically assigns drive order.

Removable Media Support

This field specifies the removable media support option for an adapter. Three settings are allowed:

None indicates no removable media support whether the drive is selected as first (BBS), or is first in the scan order (non-BBS).

Boot Drive Only provides removable media support for a removable hard drive if it is first in the scan order.

With Media Installed provides removable media regardless of the drive number assignment.

CHS Mapping

This field defines how the Cylinder Head Sector values are mapped onto a disk without pre-existing partition information. CHS Mapping allows two settings:

SCSI Plug and Play Mapping (default value) automatically determines the most efficient and compatible mapping.

Alternate CHS Mapping utilizes an alternate, possibly less efficient mapping that may be required if a device is moved between adapters from different vendors.

CAUTION

Neither of these options has any effect after a disk has been partitioned using the FDISK command. The FDISK utility is a tool that you can use to delete partition entries, one or all of them.

If all partition entries are deleted, it is necessary to reboot to clear memory or the old partitioning data will be reused, thus nullifying the previous operation. Use care to ensure that the correct disk is the target of an FDISK command.

Spinup Delay (Secs)

This field indicates the delay in seconds between spinups of devices attached to an adapter. Staggered spinups will balance the total electrical current load on the system during boot. The default value is 2 seconds, with choices between 1 and 10 seconds.

Secondary Cluster Server

This field indicates whether an adapter has one or more devices attached that are shared with one or more other adapters. If so, the SDMS SCSI BIOS should avoid SCSI Bus resets as much as possible.

This option allows you to enable an adapter to join a cluster of adapters without performing any SCSI bus resets. This is a requirement for Microsoft Cluster Server. The default value is No.

Termination Control

This field indicates whether an adapter has automatic termination control. If not available, its current status is either Auto or Off.

Auto means that the adapter automatically determines whether it should enable or disable its termination.

Off means termination at the adapter is off, and the devices at the ends of the SCSI bus must terminate the bus.

NOTE

If Auto is grayed out, it means that termination is automatic, not programmable.

Restore Defaults

To obtain default settings, press **`Enter`**.

D.4 Device Properties

The Device Properties menu allows you to view and update individual device settings for an adapter. Changing a setting for the host device (for example, SCSI ID 7) changes the setting for all devices.

The number of fields displayed requires the menu to scroll left/right in order to display the information. When accessing this menu on-line, use the Home/End keys to scroll to columns currently not displayed. The scroll indicator on the

bottom of the menu shows where the cursor is relative to the first and last columns.

Following is an example of the Device Properties menu:

Table D-6 Symbios SDMS (TM) PCI SCSI Configuration Utility Version PCI-4.19.00

Device Properties

SCSI Device Identifier	MB/Sec	MT/Sec	Data Width	Scan ID	Scan LUNs>0	Disconnect
0	[160]	[80]	[16]	[Yes]	[Yes]	[On]
1	[160]	[80]	[16]	[Yes]	[Yes]	[On]
2	[160]	[80]	[16]	[Yes]	[Yes]	[On]
3 SEAGATE ST31055N	[160]	[80]	[16]	[Yes]	[Yes]	[On]
4	[160]	[80]	[16]	[Yes]	[Yes]	[On]
5	[160]	[80]	[16]	[Yes]	[Yes]	[On]
6	[160]	[80]	[16]	[Yes]	[Yes]	[On]
7 53C1010-66	[160]	[80]	[16]	[Yes]	[Yes]	[On]
8	[160]	[80]	[16]	[Yes]	[Yes]	[On]
9	[160]	[80]	[16]	[Yes]	[Yes]	[On]
10	[160]	[80]	[16]	[Yes]	[Yes]	[On]
11	[160]	[80]	[16]	[Yes]	[Yes]	[On]
12	[160]	[80]	[16]	[Yes]	[Yes]	[On]
13	[160]	[80]	[16]	[Yes]	[Yes]	[On]
14	[160]	[80]	[16]	[Yes]	[Yes]	[On]
15	[160]	[80]	[16]	[Yes]	[Yes]	[On]

SCSI Device Identifier	SCSI Timeout	Queue Tags	Boot Choice	Format	Verify	Restore Defaults
0	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
1	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
2	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
3 SEAGATE ST31055N	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
4	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
5	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
6	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
7	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
8	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
9	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
10	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
11	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
12	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
13	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
14	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
15	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>

F1 =Help	Arrow Keys =Select Item	-/+ =Change [Item]
Esc =Abort/Exit F2 =Menu	Home/End =Select Item	Enter =Execute <Item>

D.4.1 Field Descriptions

SCSI ID

This field indicates the device's SCSI Identifier number.

Device Identifier

This field indicates the ASCII device identifier string extracted from the device's Inquiry Data.

Sync Rate (MB/Sec and MT/Sec)

MB/Sec is a field that displays information [0/ 5/ 10/ 20/ 40/ or 160]. This field indicates the maximum synchronous data transfer rate of the adapter in mega bytes per second corresponding to the width and transfer rate settings that follow.

MT/Sec is a configuration field where these values [0/ 5/ 10/ 20/ 40/ or 80] can be changed. This field indicates the maximum synchronous data transfer rate of the adapter in mega transfers per second. It can be changed to a lower transfer rate.

Data Width

This field indicates the maximum data width in bits.

Scan ID

This field indicates whether to scan for this SCSI identifier at boot time. This item can be used to ignore a device and to decrease boot time by disabling the inquiry of unused SCSI identifiers.

Set this option to "No" if there is a device that you do not want to be available to the system. Also, on a bus with only a few devices attached, the user can speed up boot time by changing this setting to "No" for all unused SCSI IDs.

Scan LUNs > 0

This field indicates whether to scan for LUNs greater than zero for a device. LUN zero is always queried. This option should be used if a multi-LUN device responds to unoccupied LUNs or if it is desired to reduce the visibility of a multi-LUN device to LUN zero only.

Set this option to "No" if you have problems with a device that responds to all LUNs whether they are occupied or not. Also, if a SCSI device with multiple LUNs exists on your system but you do not want all of those LUNs to be available to the system, then set this option to "No". This will limit the scan to LUN 0 only.

Disconnect

This field indicates whether to allow a device to disconnect during SCSI operations. Some (mostly newer) devices run faster with disconnect enabled, while some (mostly older) devices run faster with disconnect disabled.

SCSI Timeout

This field indicates the maximum amount of time [0 to 9999] in seconds to wait for a SCSI operation to complete.

Since timeouts provide a safeguard that allows the system to recover should an operation fail, it is recommended that a value greater than zero be used. A value of zero allows unlimited time for an operation to complete and could result in the system hanging (waiting forever) should an operation fail.

Press **Enter**, type in a value, and then press **Enter** again to specify a new timeout value.

Queue Tags

This field indicates whether to allow the use of queue tags for a device. Currently the BIOS does not use queue tags. This item specifies queue tag control to higher level device drivers.

Boot Choice

This field indicates whether this device may possibly be selected as the boot device. This option is only applicable to devices attached to adapter number zero (in the boot list) on non-BBS systems. It provides primitive BBS flexibility to non-BBS systems.

Format

Press **Enter** to low-level format the device. If enabled, this option allows low-level formatting on a disk drive. Low-level formatting will completely and irreversibly erase all data on the drive.

NOTE

Formatting will default the drive to a 512-byte sector size even if the drive had previously been formatted to another sector size.

Verify

Press **Enter** to verify all sectors on the device and to reassign defective Logical Block Addresses (LBAs).

Restore Defaults

Press **Enter** to obtain default settings.

D.4.2 Exiting the SCSI BIOS Configuration Utility

The Exit menu for the SCSI BIOS Configuration Utility is used for all five of the configuration menus. However, the available functionality is different for the Main menu and the four subordinate menus. Here is an example of the Exit menu:

Table D-7 Symbios SDMS (TM) PCI SCSI Configuration Utility Version PCI-4.19.00

Adapter and/or device property changes have been made		
<Cancel Exit>		
Exit the Configuration Utility		
<Save changes then exit this menu>		
<Discard changes then exit this menu>		
F1 =Help	Arrow Keys =Select Item	-/+ =Change [Item]
Esc =Abort/Exit F2 =Menu	Home/End =Select Item	Enter =Execute <Item>

To exit from the Adapter Properties, Device Properties, Boot Adapter List or Global Properties menus, use these exit options:

Cancel Exit

This option returns you to the previous menu.

Save changes then exit this menu

This option implements any changes you made on the previous menu and returns you to the Main menu.

Discard changes then exit this menu

This option restores the default settings and returns you to the Main menu.

To exit from the Main menu, use these exit options:

Cancel Exit

This returns you to the Main menu.

Exit the Configuration

This option exits the configuration utility and automatically reboots your system.

NOTE

If you reboot the system without properly exiting from this utility, some changes may not take effect.

E • Appendix E AMI BIOS Setup Utility

This appendix gives a brief description of the setup options in the system BIOS. Due to the custom nature of GE's SBCs, your BIOS options may vary from the options discussed in this appendix.

AMI refers to their BIOS setup screens as ezPORT.

To Access the First Boot setup screen press the F11 key at the beginning of boot.

To access the ezPORT setup screens, press the DEL key at the beginning of boot.

E.1 First Boot Menu

The VMIVME-7851/VME-7851RC have a First Boot menu enabling the user to, *on a one time basis*, select a drive device to boot from. This feature is useful when installing from a bootable disk. For example, when installing Windows XP from a CD, enter the First Boot menu and use the arrows keys to highlight ATAPI CD-ROM Drive. Press ENTER to continue with system boot.

This feature is accessed by pressing the F11 key at the very beginning of the boot cycle. The selection made from this screen applies to the current boot only, and will not be used during the next boot-up of the system. If you have trouble accessing this feature, disable the QuickBoot Mode in the Main BIOS setup screen. Exit, saving changes and retry accessing the First Boot menu.

Table E-1 AMI BIOS First Boot Menu

Boot Menu
1. + Removable Devices
2. + Hard Drive
3. ATAPI CD-ROM Drive
4. MBA UNDI (Bus 1 Slot 6) LAN 1
<Enter Setup>

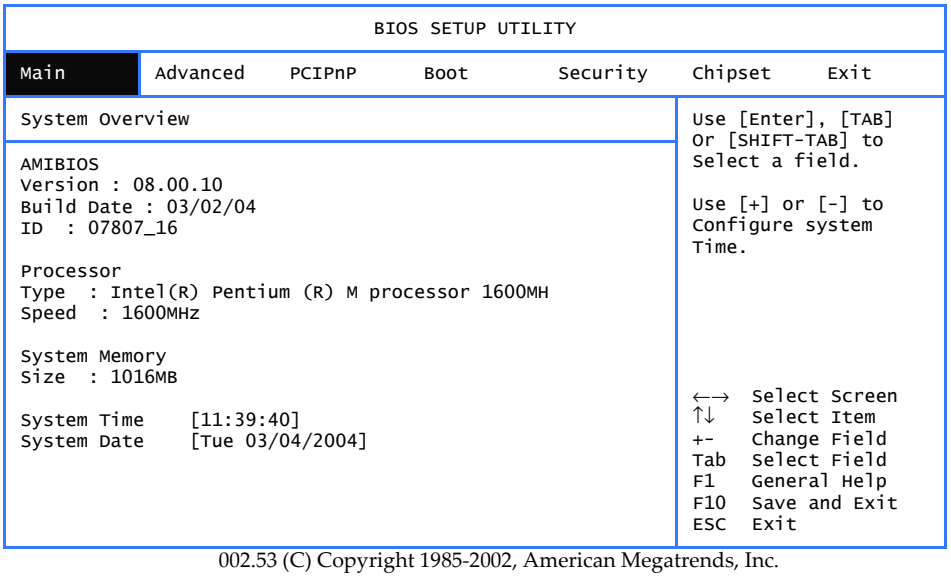
E.2 Main Menu

The Main BIOS setup menu screen has two main areas. The left frame displays all the options that can be configured. “Grayed-out” options cannot be configured. Options in blue can be configured. The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white and a text message in the right frame gives a brief description of the option.

The Main menu reports the BIOS revision, processor type and clock speed, and allows the user to set the system’s clock and calendar. Use the left and right arrow keys to select other screens.

Below is a sample of the Main screen. The information displayed on your screen will reflect your actual system.

Table E-2 AMI BIOS Main Menu



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NOTE

Options shown may not be available on your system.

E.3 Advanced BIOS Setup Menu

The Advanced BIOS Setup menu allows the user to configure some CPU settings, the IDE bus, SCSI devices, other external devices and internal drives.

Select the *Advanced* tab from the ezPORT setup screen to enter the Advanced BIOS Setup screen. You can select the items in the left frame of the screen, such as Super I/O Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. A sample of the Advanced BIOS Setup screen is shown below.

NOTE

Changes in this screen can cause the system to malfunction. If problems are noted after changes have been made, reboot the system and access the BIOS. From the Exit menu select '`Load Failsafe Defaults`' and reboot the system. If the system failure prevents access to the BIOS screens, refer to ***To Clear the CMOS Password:*** on page 111 for instructions on clearing the CMOS.

Table E-3 AMI BIOS Advanced Menu

```
                              BIOS SETUP UTILITY
Main | Advanced | PCIPnP | Boot | Security | Chipset | Exit

Advanced Settings                                  Configure CPU.

WARNING: Setting wrong values in below sections
         may cause system to malfunction.

➢  CPU Configuration
➢  IDE Configuration
➢  Floppy Configuration
➢  SuperIO Configuration
➢  Remote Access Configuration
➢  USB Configuration

                                                   ←→   Select Screen
                                                   ↑↓   Select Item
                                                   Enter Go to Sub Screen
                                                   F1   General Help
                                                   F10  Save and Exit
                                                   ESC  Exit
```

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NOTE

Options shown may not be available on your system.

E.4 PCI/PnP Setup Menu

Included in this screen is the control of internal peripheral cards, as well as various interrupts. From this menu, the user can also determine if the system's plug-and-play is enabled or disabled.

NOTE

Changes in this screen can cause the system to malfunction. If problems are noted after changes have been made, reboot the system and access the BIOS. From the Exit menu select '`Load Failsafe Defaults`' and reboot the system. If the system failure prevents access to the BIOS screens, refer to ***To Clear the CMOS Password:*** on page 111 for instructions on clearing the CMOS.

Below is a sample screen of the PCI/PnP menu; options in your system may be different from those shown.

Table E-4 AMI BIOS PCI/PnP Menu

```
                              BIOS SETUP UTILITY
Main      Advanced   PCIPnP   Boot      Security   Chipset   Exit

Advanced PCI/PnP Settings                          NO: lets the BIOS configure all the
                                                   devices in the system. YES: lets the
WARNING: Setting wrong values in below sections    operating system configure Plug and
         may cause system to malfunction.          Play (PnP) devices not required for
                                                   boot if your system has a Plug and
Plug & Play O/S                    [Yes]           Play operating system.
PCI Latency Timer                  [64]
Allocate IRQ to PCI VGA            [Yes]
Palette Snooping                   [Disabled]
PCI IDE BusMaster                  [Disabled]
OffBoard PCI/ISA IDE Card          [Auto]

IRQ3                               [Available]
IRQ4                               [Available]
IRQ5                               [Available]     ←→   Select Screen
IRQ7                               [Available]     ↑↓   Select Item
IRQ9                               [Available]     +-   Change Option
IRQ10                              [Available]     F1   General Help
IRQ11                              [Available]     F10  Save and Exit
IRQ14                              [Available]     ESC  Exit
```

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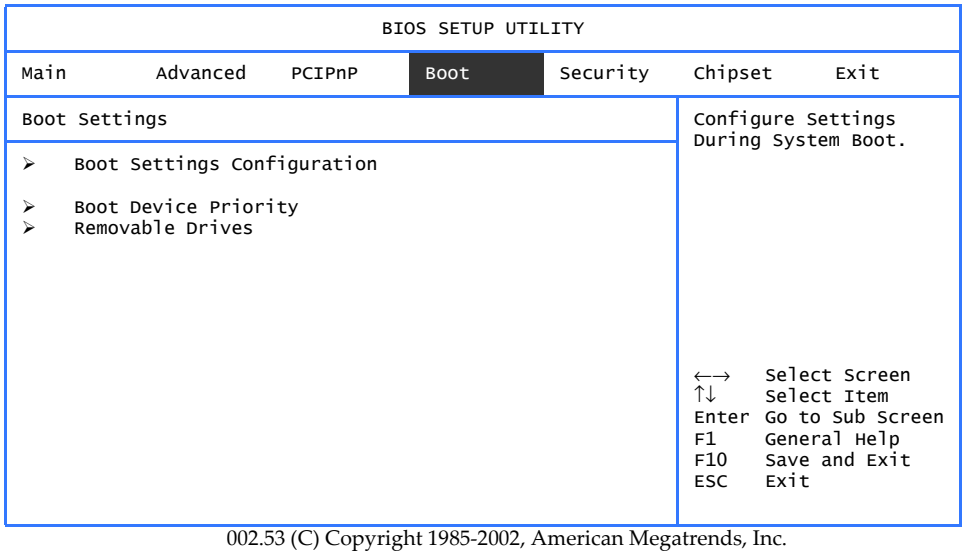
E.5 Boot Setup Menu

Use the Boot Setup menu to set the priority of the boot devices, including booting from a remote network. The devices shown in this menu are the bootable devices detected during POST. If a drive is installed that does not appear, verify the hardware installation. Also available in this screen are “Boot Settings” which allow the user to set how the basic system will act, for example, support for PS/2 mouse and whether to use “Quick Boot” or not.

Table E-5 AMI BIOS Boot Menu



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E.6 Security Setup Menu

The ezPORT setup provides both a Supervisor and a User password. If you use both passwords, the Supervisor password must be set first.

The system can be configured so that all users must enter a password every time the system boots or when ezPORT setup is executed, using either the Supervisor password or User password.

Table E-6 AMI BIOS Security Menu

BIOS SETUP UTILITY						
Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

Security Settings	Install or Change the password.
Supervisor Password : Not Installed User Password : Not Installed Change Supervisor Password Change User Password Clear User Password Boot Sector Virus Protection [Disabled]	←→ Select Screen ↑↓ Select Item Enter Change F1 General Help F10 Save and Exit ESC Exit

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To reset the security in the case of a forgotten password you must drain the NVRAM and reconfigure.

E.6.1 To Clear the CMOS Password:

1. Turn off power to the unit.
2. Momentarily short pins of E3 for approximately five seconds
3. Power up the unit.

When the power is reapplied to the unit, the CMOS password will have been cleared, and the CMOS will be set to its defaults.

E.7 Chipset Setup Menu

Select the various options for chipsets located in the system (for example, the CPU configuration and configurations for the North and South Bridge). The settings for the chipsets are processor dependent and care must be used when changing settings from the defaults set at the factory. Below is a sample of the Chipset Setup screen; the actual options on your system may vary.

NOTE

Changes in this screen can cause the system to malfunction. If problems are noted after changes have been made, reboot the system and access the BIOS. From the Exit menu select 'Load Failsafe Defaults' and reboot the system. If the system failure prevents access to the BIOS screens, refer to ***To Clear the CMOS Password:*** on page 111 for instructions on clearing the CMOS.

Table E-7 AMI BIOS Chipset Menu

```
                                BIOS SETUP UTILITY
Main      Advanced    PCIPnP    Boot      Security  Chipset   Exit

Advanced Chipset Settings                          Intel Montara GML
                                                   NorthBridge chipset
WARNING: Setting wrong values in below section     Configuration options.
         may cause system to malfunction.

➢  NorthBridge Configuration
➢  SouthBridge Configuration
➢  CPCI (HINT HB6) Bridge Configuration
➢  Lan (8254EB) Port Routing Options

                                                   ←→   Select Screen
                                                   ↑↓   Select Item
                                                   Enter Go to Sub Screen
                                                   F1   General Help
                                                   F10  Save and Exit
                                                   ESC  Exit
```

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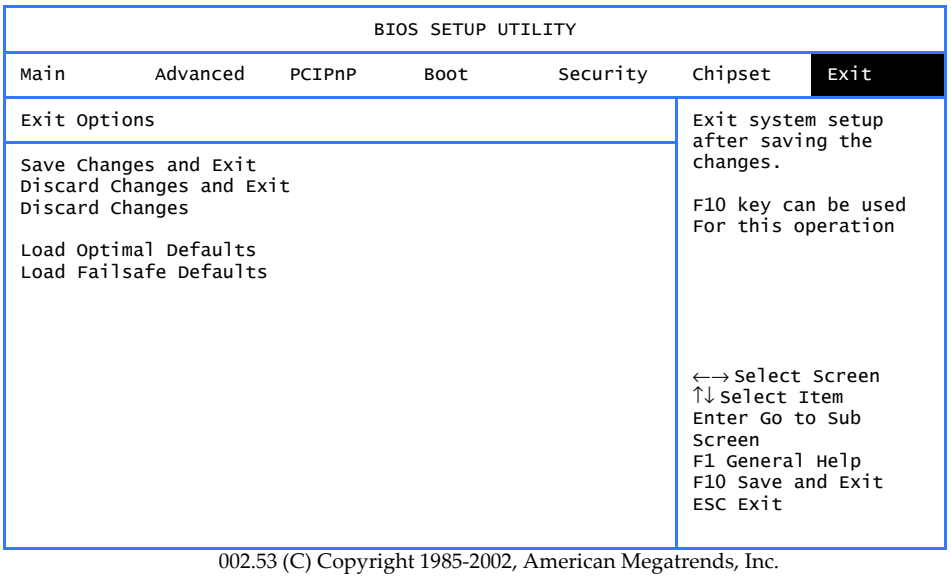
E.8 Exit Menu

Select the *Exit* tab from the ezPORT setup screen to enter the Exit BIOS Setup screen. You can display an Exit BIOS Setup option by highlighting it using the <Arrow> keys. The Exit BIOS Setup screen is shown below.

Table E-8 AMI BIOS Exit Menu



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If changes have previously been made in the BIOS and the system malfunctions, reboot the system and access this screen. Select “Load Failsafe Defaults” and continue the reboot.

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Additional Resources

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