GE Fanuc Automation

VMIPCI-5565 Specifications

Ultrahigh Speed Fiber-Optic Reflective Memory with Interrupts

Features:

- High speed, easy to use fiber-optic network (2.12 Gbaud serially)
- Data written to memory in one node is also written to memory in all nodes on the network
- Up to 256 nodes
- Connection with multimode fiber up to 300m, single mode fiber up to 10km
- Dynamic packet size, 4 to 64 bytes of data
- Transfer rate 47.1MB/s (4 byte packets) to 174MB/s (64 byte packets)
- 64MB or 128MB SDRAM Reflective Memory
- Two independent DMA channels
- Any node on the network can generate an interrupt in any other node on the network or in all network nodes with a single command
- Error detection
- Redundant transfer mode for extra error suppression
- No processor overhead
- No processor involvement in the operation of the network
- PCI 64-bit 66MHz transfers
- PCI revision 2.2 compliant
- VMISFT-RFM2g network and shared memory driver included
- Operating system/driver support for Windows NT®, Windows® 2000, VxWorks®, and Linux®

GE FANUC

Embedded Systems

Ordering Options							
July 16, 2007 800-855565-000 G		A	B	C	D	E	F
VMIPCI-5565	–		1		0	0	

A = Memory Options
0 = 64MB
1 = 128 MB
B = FIFOs
0 = Reserved
1 = 4 K FIFOs
C = Transmission Mode
0 = Multimode
1 = Single Mode
DE = 0 (Options reserved for future use)
F = Conformal Coating
0 = No Conformal Coating
1 = Conformal Coating

Simplex Cable Specifications

Fiber-Optic Cable – Multimode; (62.5 Micron core)

Fiber-Optic Cable Assemblies		A	B	C
VMICBL-000-F5	–	0		

ABC = Cable Lengths

000 = .5 ft (0.15m)	011 = 350 ft (106.68m)
001 = 1 ft (.31m)	012 = 500 ft (152.15m)
002 = 5 ft (1.52m)	013 = 574 ft (175m)
003 = 10 ft (3.04m)	014 = 656 ft (200m)
004 = 25 ft (7.62m)	015 = 820 ft (250m)
005 = 50 ft (15.24m)	016 = 1,000 ft (304.30m)
006 = 80 ft (24.40m)	017 = 1,148 ft (350m)
007 = 100 ft (30.49m)	018 = 1,312 ft (400m)
008 = 150 ft (45.72m)	019 = 1,500 ft (456.45m)
009 = 200 ft (60.98m)	020 = 1,640 ft (500m)
010 = 250 ft (76.20m)	

For Ordering Information, Call:
1-800-322-3616 or 1-256-880-0444 • FAX (256) 882-0859
Email: info.embeddedsystems@gefanuc.com
Web Address: www.gefanucembedded.com

Functional Characteristics

Introduction: VMIPCI-5565 is the PCI member of the GE Fanuc Embedded Systems' VMIxxx-5565 family of Reflective Memory (RFM) real time network products. The other members of the family are VMIVME-5565, VME-compatible board, and VMIPMC-5565, the PCI mezzanine card (PMC). All three of these products are network compatible, and may be integrated into a network in any combination.

This family of products allows computers, workstations, PLCs, and other embedded controllers with dissimilar operating systems or no operating system at all to share data in real time.

To the local node, the Reflective Memory board appears as shared memory. Data can be written to or read from the memory by any level of software, including the application itself. Data written to the Reflective Memory in one node is transported by the network hardware to all other nodes and placed in the same address on those node's Reflective Memory boards. This transport of data is accomplished without the involvement of the processors on any node. By this system, all nodes on the network have a local copy of shared data available for immediate access.

Product Overview: The Reflective Memory concept provides a very fast and efficient way of sharing data across distributed computer systems.

The VMIPCI-5565 Reflective Memory interface allows data to be shared between up to 256 independent systems (nodes) at rates up to 174MB/s. Each Reflective Memory board may be configured with 64MB or 128MB of onboard SDRAM. The local SDRAM provides fast Read access times to stored data. Writes are stored in local SDRAM and broadcast over a high speed fiber-optic data path to other Reflective Memory nodes. The transfer of data between nodes is software transparent, so no I/O overhead is required. Transmit and Receive FIFOs buffer data during peak data rates to optimize the host computer and bus performance to maintain high data throughput.

The Reflective Memory also allows interrupts to one or more nodes by writing to a byte register. These interrupt (four levels, each user definable) signals may be used to synchronize a system process, or used to follow any data. The interrupt always follows the data to ensure the reception of the data before the interrupt is acknowledged.

Each node on the system has a unique identification number between 0 and 255. The node number is established during hardware system integration by placement of jumpers on the board. This node number can be read by software by accessing an onboard register. In some applications, this node number would be useful in establishing the function of the node.

Link Arbitration: The VMIPCI-5565 system is a fiber-optic daisy chain ring as shown in Figure 2. Each transfer is passed from node-to-node until it has gone all the way around the ring and reaches the originating node. Each node retransmits all transfers that it receives except those that it originated. Nodes are allowed to insert transfers between transfers passing through.

Interrupt Transfers: The VMIPCI-5565 provides four network interrupts. Any processor can generate an interrupt on any other node on the network. In addition, any processor can generate an interrupt on all nodes on the network with a single register write.

In response to this interrupt register write, the sending VMIPCI-5565 issues a special packet over the network, which contains the command strobe, the sender node ID, the destination node ID, and 32 bits of data. When a receiving node detects the proper combination of destination node ID and command strobe, it stores the sender note ID and the data in one of four 127 location-deep FIFOs. The four FIFOs correspond to the four interrupts. Upon storing this information in a FIFO, the receiving node issues an interrupt to the local processor if it has been software-enabled. The 32 bits of data stored in the FIFO is user-definable and typically is treated as an interrupt vector. As part of an interrupt service routine, the local processor reads this information out of the FIFO and acts accordingly.

PCI Initiator/Direct Memory Access (DMA) Capabilities: The VMIPCI-5565 supports DMA operations. The DMA sequence is initialized by a few control register writes to the VMIPCI-5565 by the host. Therefore, the VMIPCI-5565 becomes a PCI initiator and moves the specified block of data up to 64MB without further host attention. The PCI architecture ensures that the VMIPCI-5565 does not monopolize the PCI bus and causes the VMIPCI-5565's DMA engine to automatically split large blocks in small bursts. The VMIPCI-5565 can be programmed to issue a PCI interrupt upon completion of DMA process. There are two independent DMA engines, each capable of reading or writing. It is possible for a Read DMA and a Write DMA to occur simultaneously.

Error Management: Errors are detected by the VMIPCI-5565 with the use of the error detection facilities of the Fibre Channel encoder/decoder and additional cyclic redundant encoding and checking. When a node detects an error, the erroneous transfer is removed from the system and an interrupt is generated, if enabled.

Protection Against Lost Data: The product is designed to prevent either FIFO from becoming full and overflowing. It is important to note the only way that data can start to accumulate in FIFOs is for data to enter the node at a rate greater than the network data rate. Since data can enter from the fiber and from the PCI bus, it is possible to exceed these rates. If the transmit FIFO becomes half-full, a bit in the Status Register is set. This is an indication to the node's software that subsequent WRITEs to the Reflective Memory should be suspended until the FIFO is less than half-full. Once the transmit FIFO is almost full, writes to the Reflective Memory will be acknowledged with a STOP*. No data will be lost.

If the receive FIFO is allowed to become almost full, there is a danger the receiver FIFO may overflow resulting in data loss. In order to prevent this situation, all PCI writes will be acknowledged by a STOP* until the receiver FIFO is less than almost full.

Redundant Transfer Mode: The VMIPCI-5565 can optionally be placed in the redundant transfer mode by the removal of a board jumper shunt. While in the redundant transfer mode, each packet sent on the network by the transmitter is sent twice, regardless of the dynamic packet size. The receiving circuitry of each node on the network evaluates each of the redundant transfers. If no errors are detected in the first transfer, it is used to update the onboard memory and the second transfer is discarded. If, however, the first transfer does not contain an error, the second transfer is used to update the onboard memory provided it has no transmission error. In the remote chance that both redundant transfers contain an error, neither transfer is used and the data is completely removed from the network.

The redundant transfer mode greatly reduces the chance that any data is dropped from the network. However, the redundant transfer mode also reduces the effective network transfer rates. The single Lword (4 byte) transfer rate drops to approximately 20MB/s. The 16 Lword (64 byte) transfer rate drops to the redundant rate of 87MB/s.

Network Monitor: There is a bit in a Status Register that can be used to verify that data is traversing the ring (that is, the ring is not broken). This can also be used to measure network latency.

VMISFT-RFM2g Network and Shared Memory Driver: The VMISFT-RFM2g network and shared memory driver provides an applications program with three convenient methods for exchanging data among hosts connected to the same RFM network:

1) **Programmed I/O (Peek and Poke):** An applications program can treat the memory on the RFM device as ordinary memory in which the program can use ordinary load and store accesses.

2) **DMA:** On systems where the performance penalty for individual bus accesses is unacceptably high, the driver utilizes the DMA feature available on some RFM devices in order to transfer data in variable-sized blocks. On UNIX systems, an applications program uses the familiar `lseek(2)/read(2)/write(2)` system calls to perform the data movement, while on other operating systems a GE Fanuc Embedded Systems-provided application program interface (API) is used for data movement.

3) **User Interrupts:** The VMIPCI-5565 provides three network interrupts. Any processor can generate an interrupt on any other node on the network. In addition, any processor can generate an interrupt on all nodes on the network with a single register write.

Specifications

Memory Size: 64 or 128 MB

PCI Transfer Rate: 264 MB/s (33MHz/64-bit bus) or 528MB/s (66MHz/64-bit bus)

Throttles back to available link data rate as FIFOs begin to fill

Transfer Specification

Network Nonredundant Transfer Rate: 47.1MB/s (single longword accesses) to 174MB/s (64 byte bursts)

Network Redundant Transfer Rate: 20MB/s (single longword accesses) to 87MB/s (64 byte bursts)

Cables

Multimode Fiber Cable: Small form factor (SFF)
850nm, 970 ft, multimode LC connector

Single Mode: Small form factor (SFF)
1,300nm, single mode, 10km or 6.21 miles

Physical/Environmental Specifications

Power Requirements:
+3.3VDC (±5 percent), 1.5A maximum

Temperature:
Operating: 0 to +65° C with forced air cooling
Storage: -40 to +85° C

Relative Humidity: 20% to 80%, noncondensing

MTBF: Contact factory

Regulatory: The VMIPCI-5565 has been tested to and found to meet the requirements of the following standards.

European Union (CE Mark)
EN55024
EN55022 Radiated Emissions Class B
EN61000-4-2 (ESD)
EN61000-4-3 (Radiated Immunity)
EN61000-4-4 (EFT)
EN61000-4-5 (Surge)
EN61000-4-6 (Conducted RF)

United States
FCC Part 15, Class B

Canada
ICES-003, Class B

Data Transfers

Data written into the Reflective Memory is broadcast to all nodes on the network without further involvement of the sending or receiving nodes. Data is transferred from memory locations on the sending nodes to corresponding memory locations on the receiving nodes.

A functional block diagram of the VMIPCI-5565 is shown in Figure 1 and a network example using Reflective Memory in Figure 2.

Trademarks

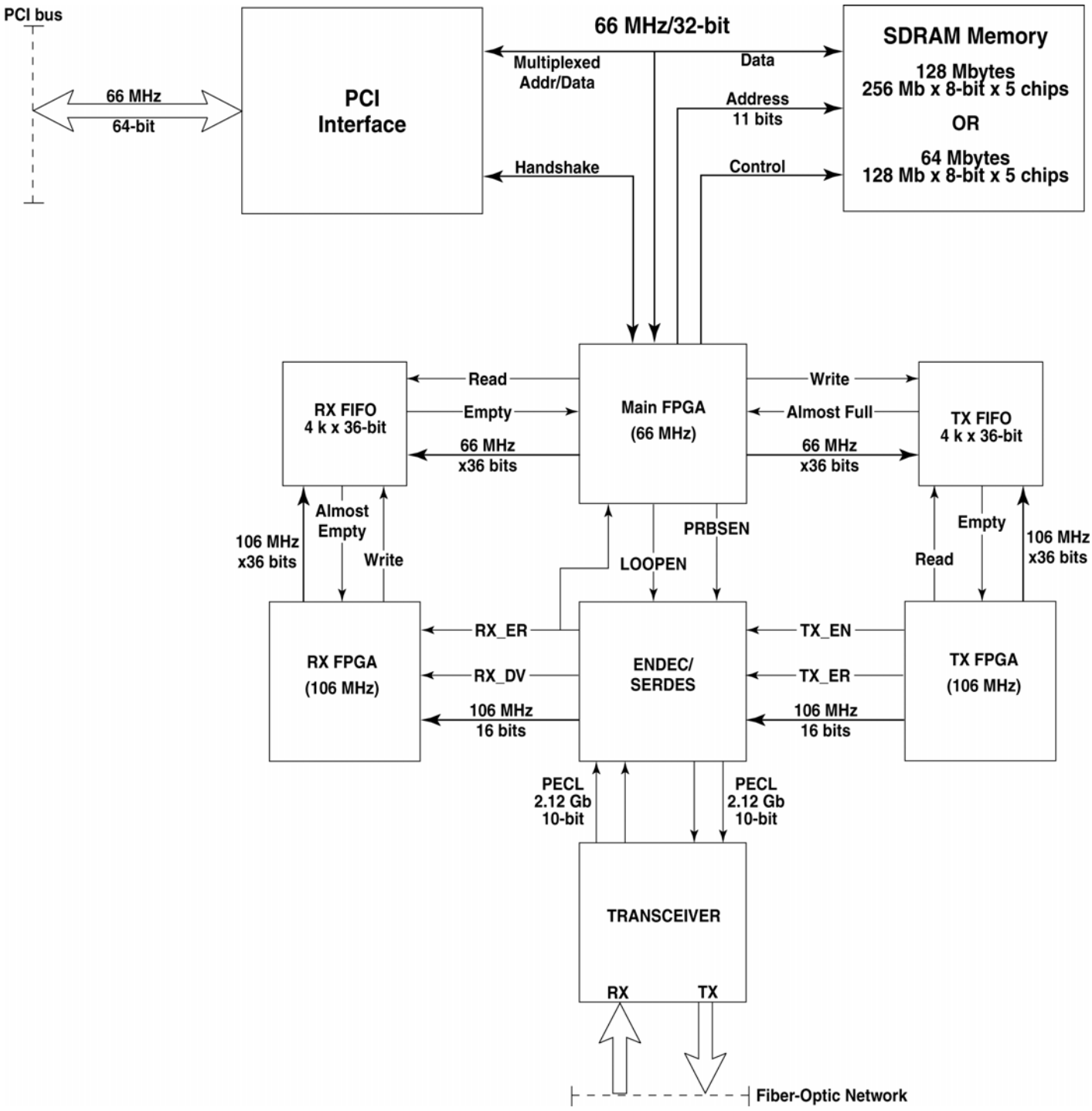

Figure 1. VMIPCI-5565 Functional Block Diagram

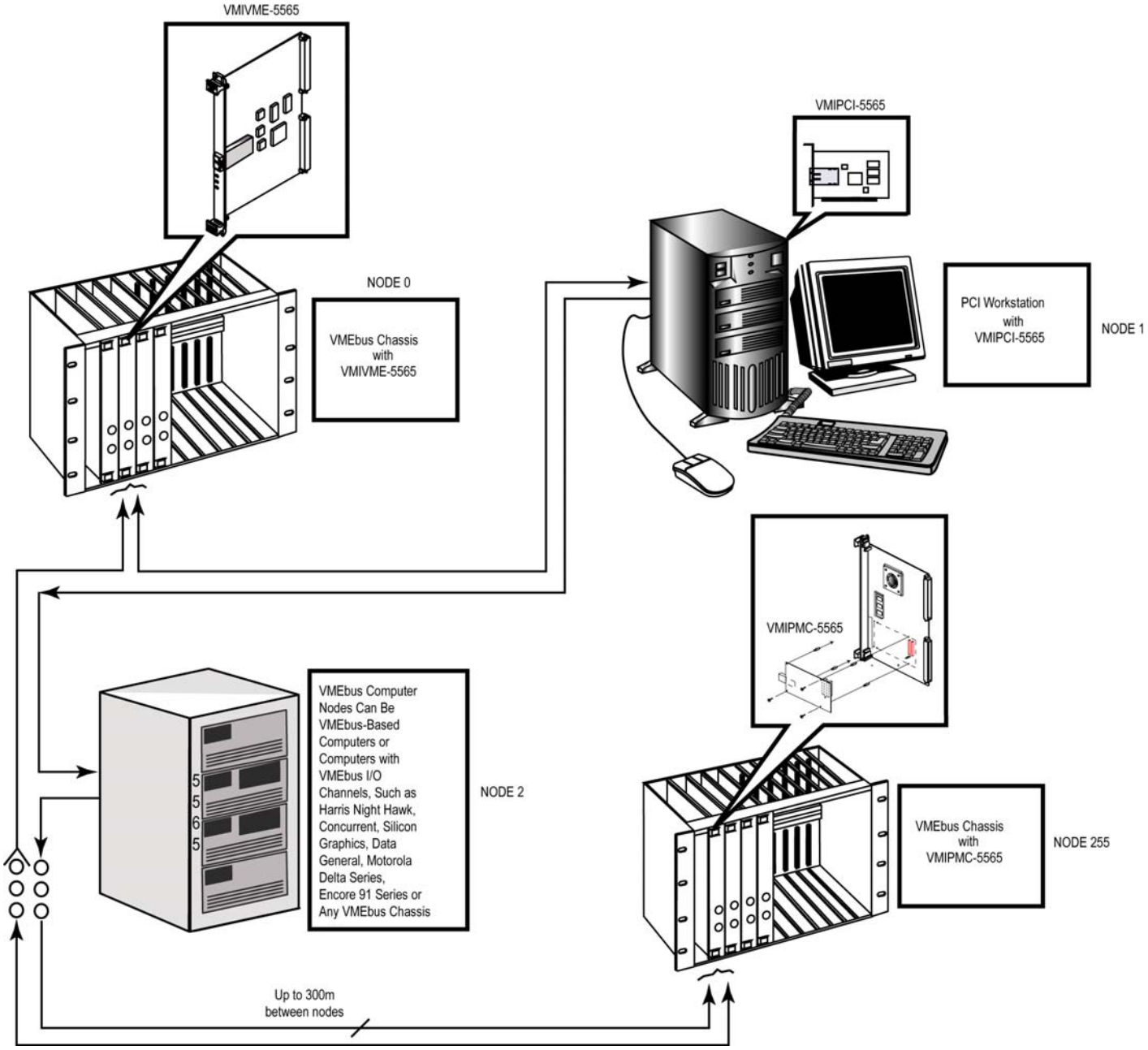

Figure 2. Network Example Using Reflective Memory System

GE Fanuc Embedded Systems Information Centers

Americas:
Huntsville, AL 1 800 322-3616
1 (256) 880-0444
Camarillo, CA 1 (805) 987-9300
Greenville, SC 1 (864) 627-8800

Europe, Middle East and Africa:
Edinburgh, UK 44 (131) 561-3520
Paris, France 33 (1) 4324 6007

Additional Resources

For more information, please visit the GE Fanuc Embedded Systems web site at:
www.gefanucembedded.com